ETHERNET ATTACHED TFT PROJECT
DISPLAY CONTROLLER MODULE

SCHEMATIC DIAGRAMS

REVISION 0.3

AUGUST 2006

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Revision history

0.3 (2006-08-30)

- Added oscillator as a clock source for video controller

0.2 (2006-08-29)

- Added diagram of the internal structure of the controller - inside FPGA

0.1 (2006-08-28)

- Initial revision

Block diagram

External connections

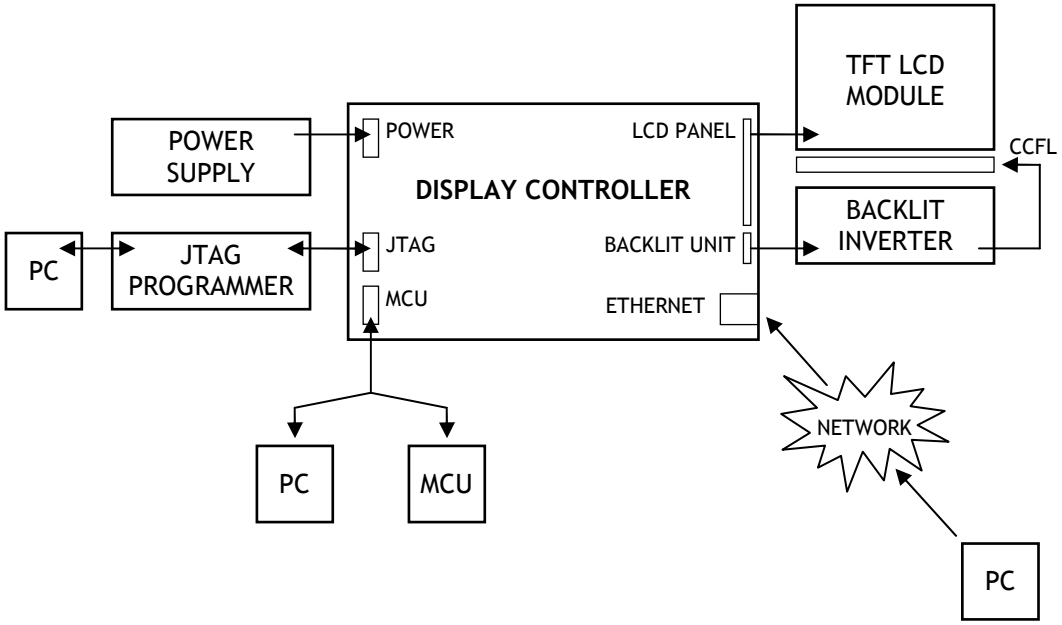

Fig.1: External connections to the display controller

Internal structure

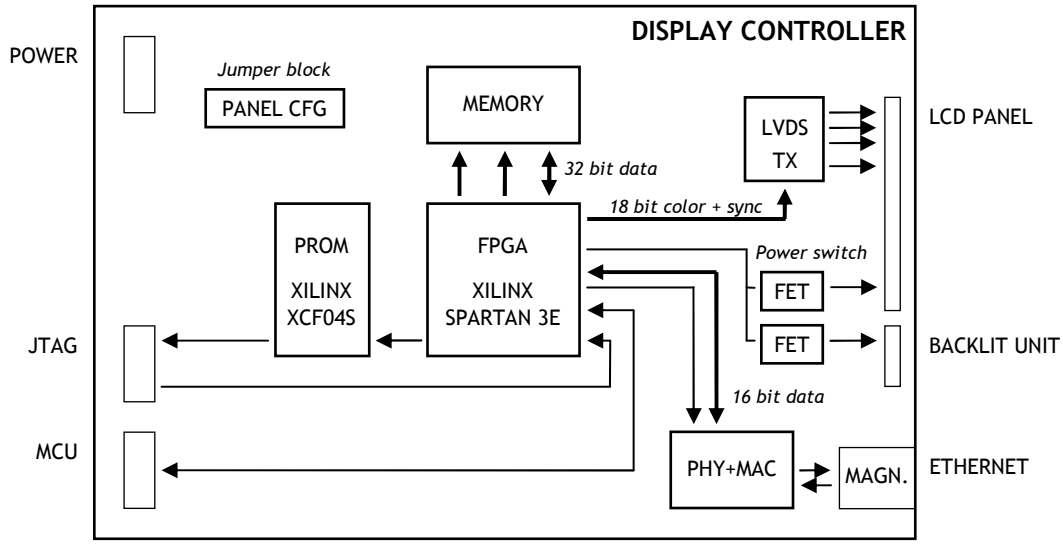

Fig.2: Internal structure of the display controller

Detailed schematics

Power input

The power supply is located externally, connected using a 10 wire flat cable.

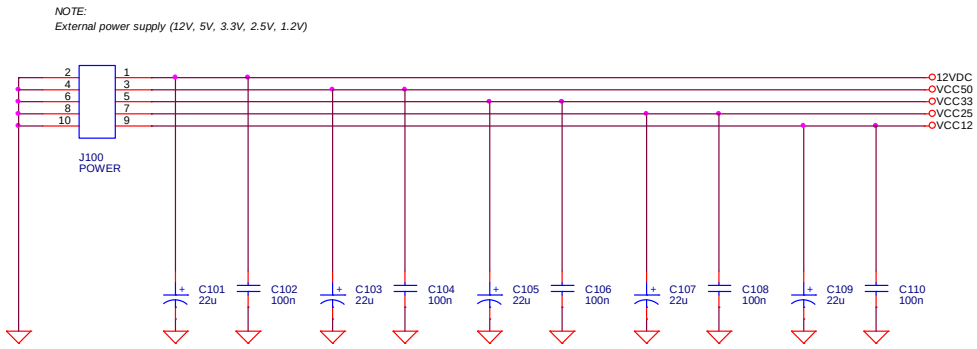

Fig.3: Power input connector and filtering capacitors

Required power:

- Unstabilized
  - 12V – backlit power
- Stabilized
  - 1.2V – FPGA core
  - 2.5V – JTAG chain
  - 3.3V – FPGA input/output pins, Ethernet, memory, LVDS, TFT panel
  - 5.0V – backlit on/off control

FPGA

Power

JTAG chain is powered by V_{CCAUX} = 2.5V and the internals (core) runs with V_{CCINT} = 1.2V. Input/output banks are configured to use V_{CCO} = 3.3V.

A decoupling capacitor is placed next to each power input pin.

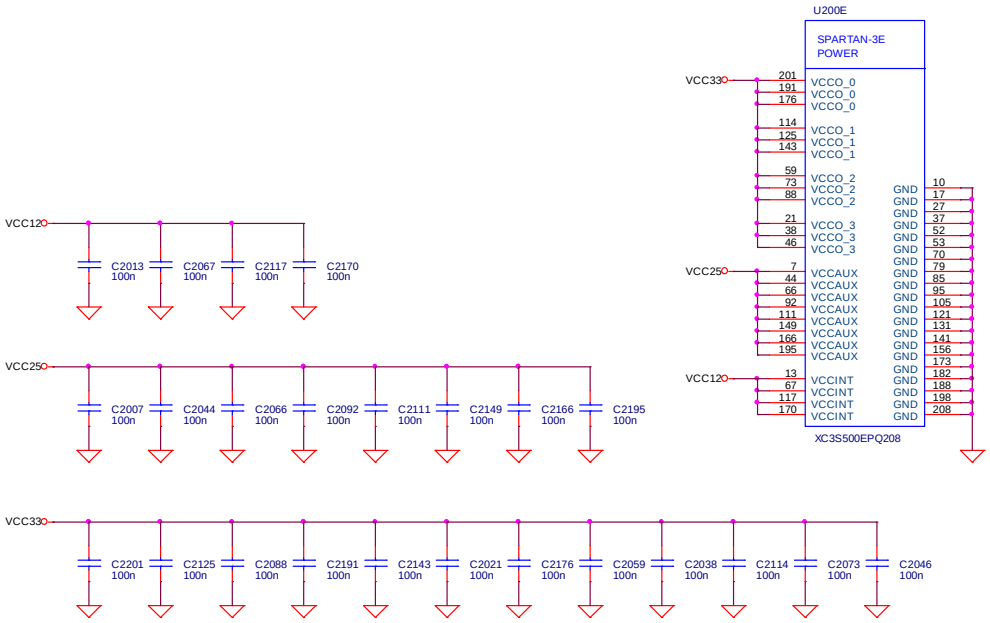

Fig.4: FPGA power distribution

Configuration

The configuration PROM input/output runs on V_{CCO} = 3.3V.

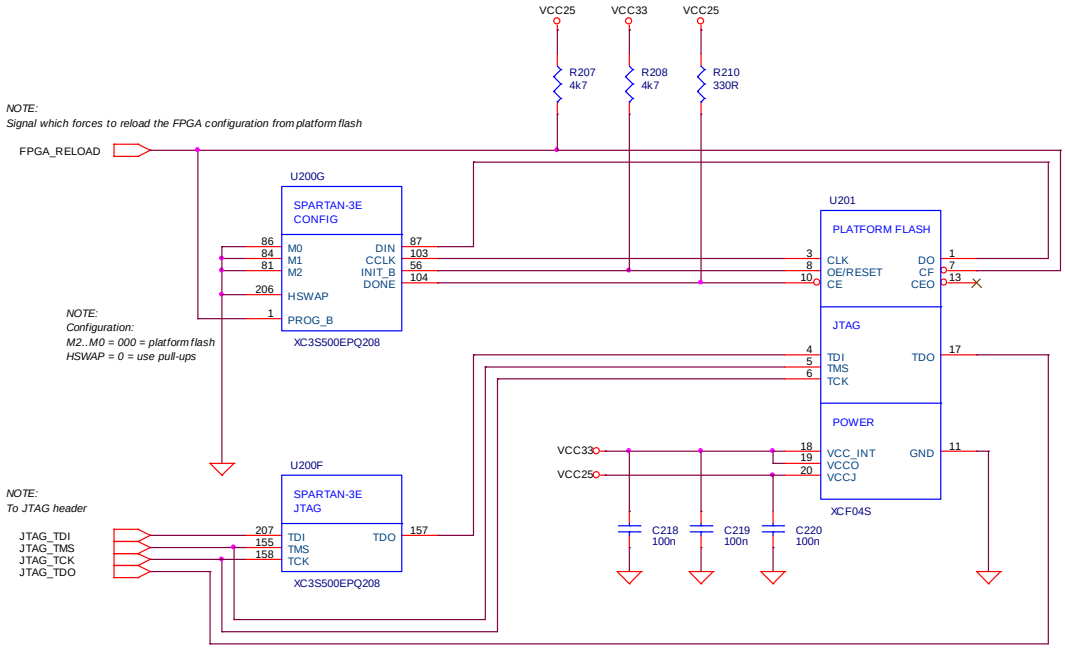

Fig.5: FPGA configuration PROM and JTAG chain

IO pins

The preliminary distribution of input/output pins (the exact assignment of pins can change with the PCB design phase):

- Memory: top and right edge
- Ethernet: left edge
- Display data (to LVDS): bottom edge
- Microcontroller: top-left corner

Free (unused) input/output pins: 2 (IO44, IO55).

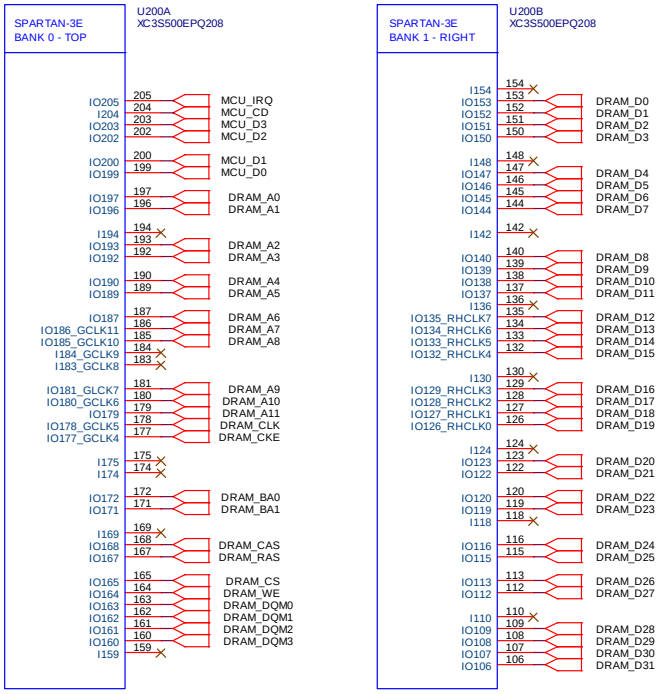

Fig.6: Top and right edge

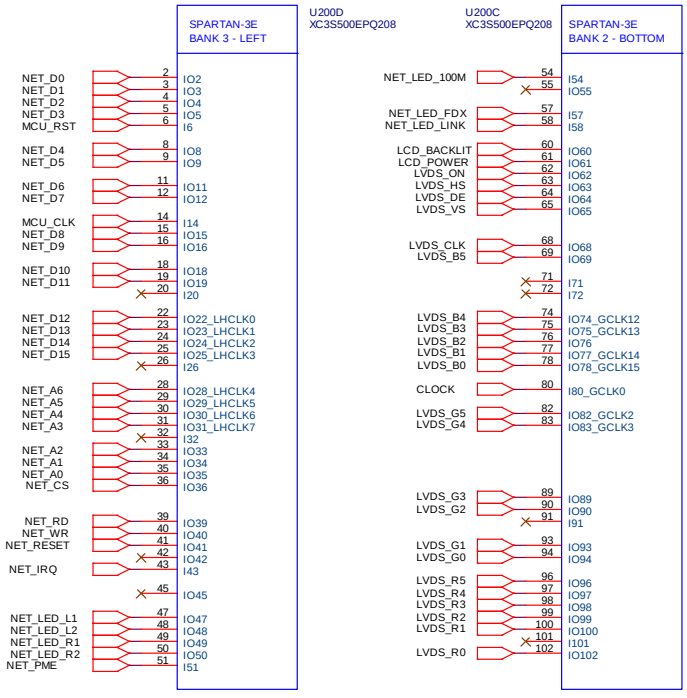

Fig.7: Left and bottom edge

Ethernet

The LAN9218I integrated PHY/MAC is connected to FPGA using a 16 bit bus and uses an external EEPROM memory to store the physical address (MAC address) of the device.

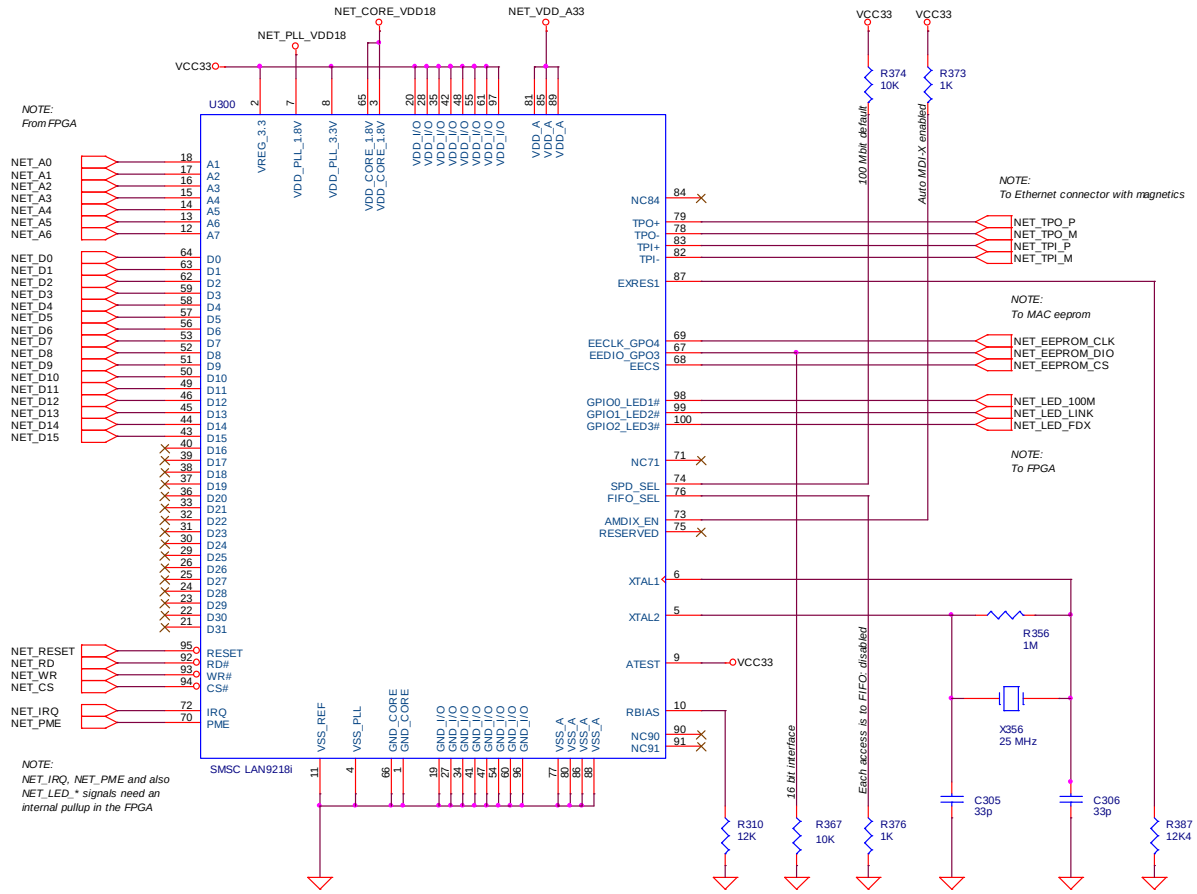

Fig.8: Integrated PHY/MAC with configuration setup

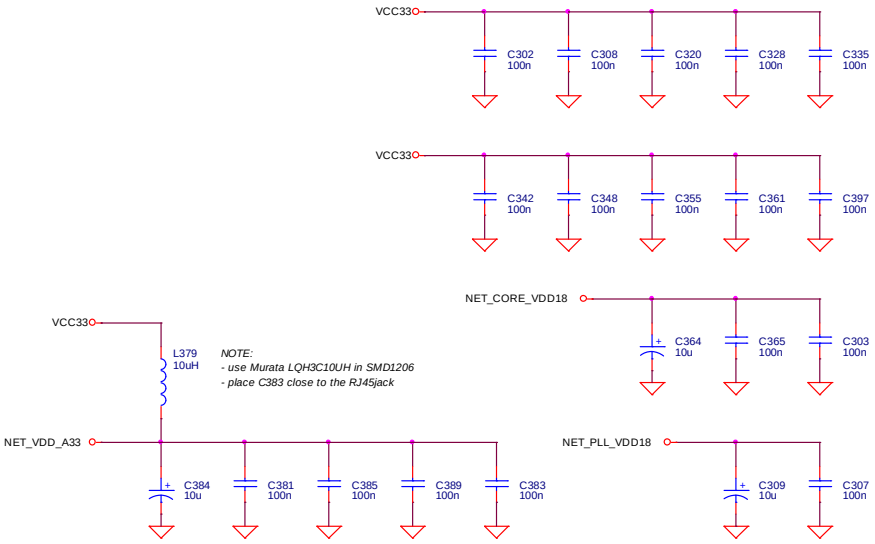

Fig.9: Network controller decoupling capacitors

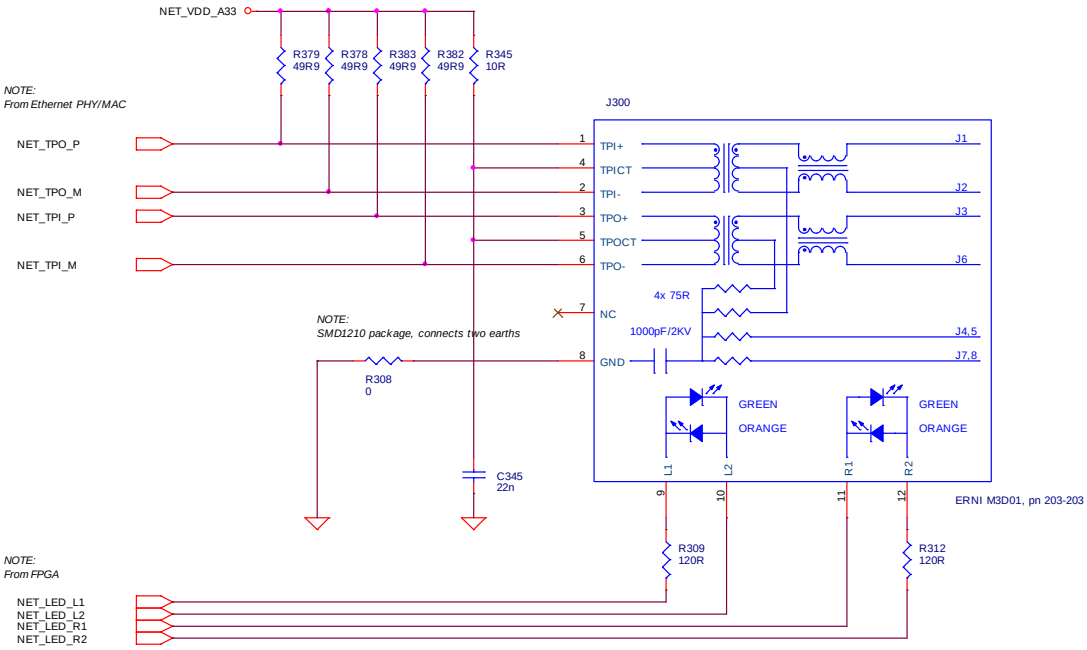

Fig.10: The RJ45 with integrated magnetics

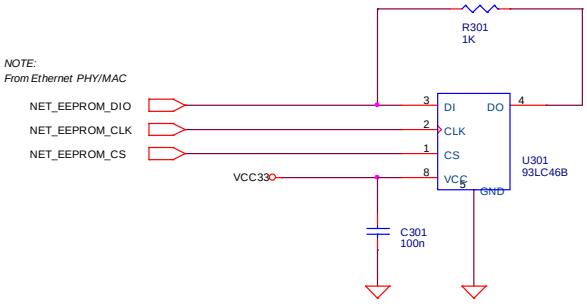

Fig.11: Network configuration EEPROM

Display module

The only supported display module is an 18-bit color TFT panel. The power options of the panel and backlit inverter can be configured with jumpers as follows:

Parameter	Available options
TFT module power	**3.3V**
	5V
Backlit power	5V
	12V
Backlit on/off signal level	**0/5V**
	0/12V
Backlit brightness adjustment signal level	**0...5V**
	0...12V

LVDS transmitter

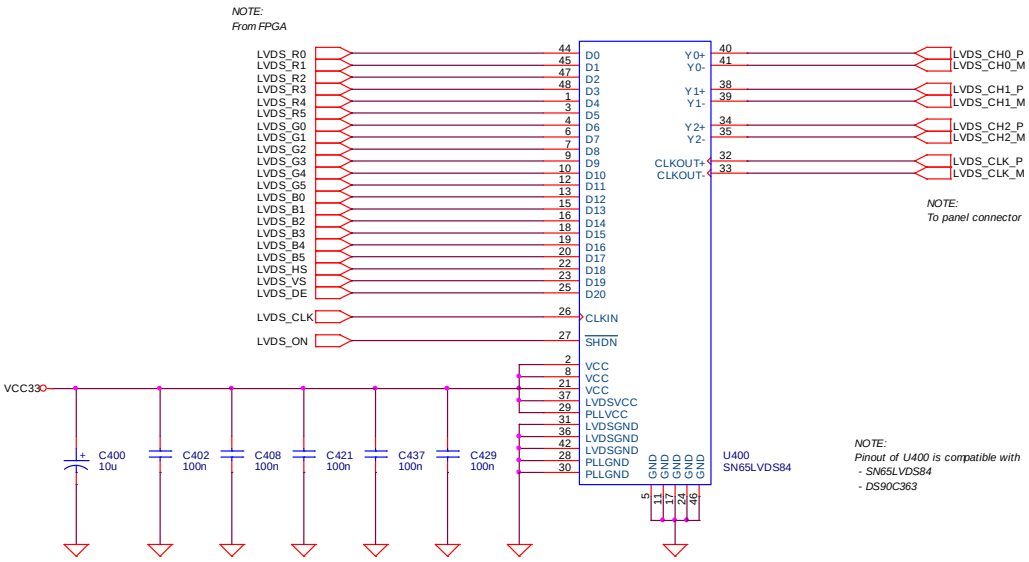

Fig.12: An 18-bit LVDS transmitter with decoupling capacitors

LCD module port

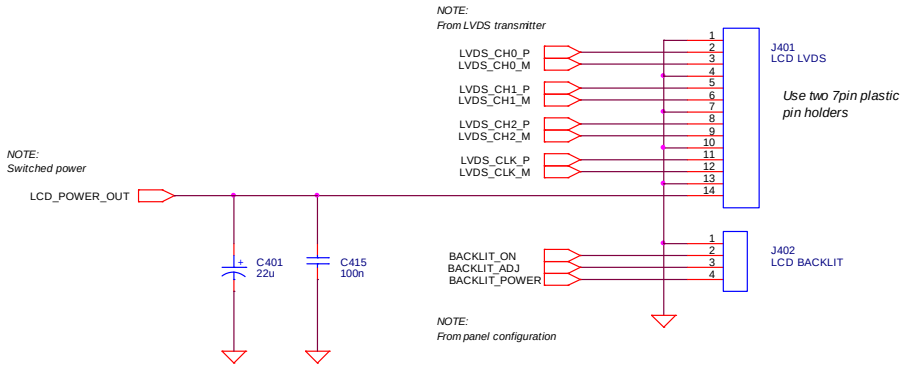

Fig.13: TFT panel and backlit connectors

Configuration

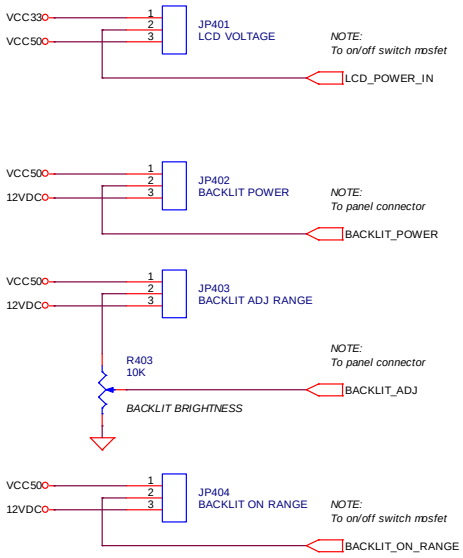

Fig.14: Jumpers to set the TFT power configuration

Power switching

TFT module datasheets use to show a powering sequence (panel, LVDS, backlit) and these switches allow fulfilling this requirement.

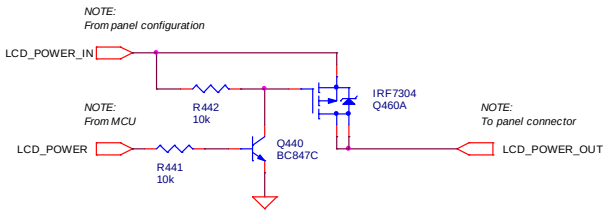

Fig.15: Switch for the TFT panel's power line

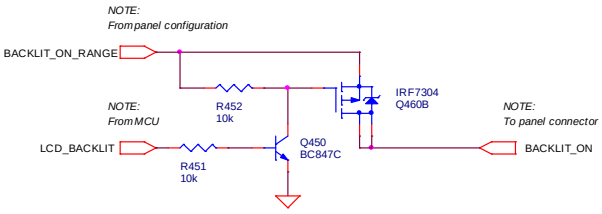

Fig.16: Switch for the backlit unit's on/off signal

Memory

The two chip configuration is used to obtain wider data path.

Parameters:

- 2x16 bit data = 32 bit data path
- 4 banks with 1Mx16 (twice) = 16MB total memory
- used chips are from 100MHz SDRAM DIMM
- peak data rate: 400MB/s

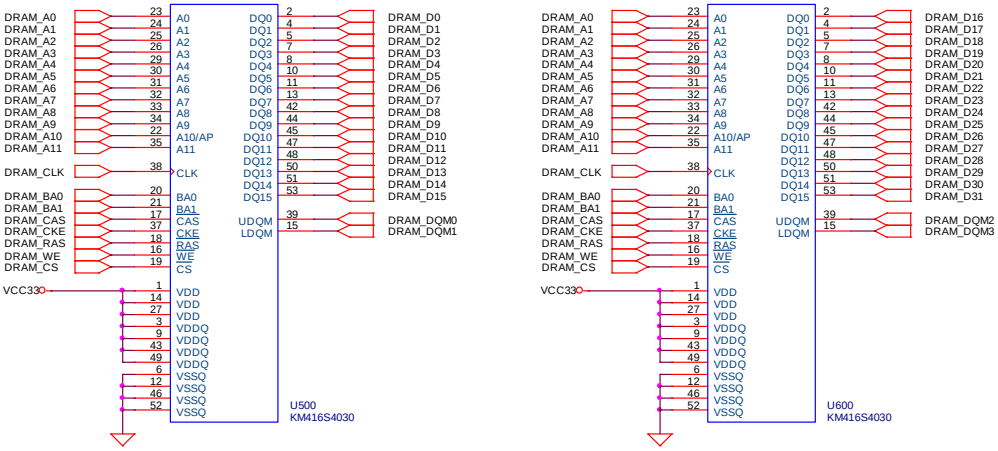

Fig.17: Two memory chips

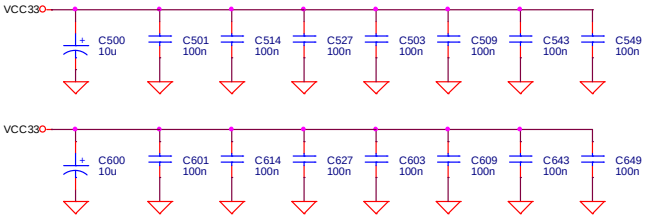

Fig.18: Decoupling capacitors for each power pin of memory

Clock source

The standalone crystal oscillator is used as a clock source for the video controller.

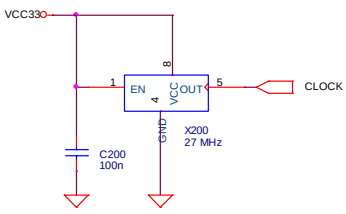

Fig.19: Video controller clock source

Microcontroller port

The microcontroller port is composed using the free input/output pins of FPGA. The communication is done using a 4 bit wide words which can be transferred in multiple cycles to get over larger data.

Hardware

The 47Ω resistors are used to limit the current when connecting to a 5V device (the voltage on the input/output pin of FPGA is limited to about 3.8V using clamping diodes, but the pin itself should not be stressed with more than 100mA. Using the specified resistors, the worst case current is 25.5 mA at 5V on MCU PORT).

The preferred logic types on the MCU PORT are:

- 3.3V CMOS
- open collector with pull-up resistors to 3.3V
- 5V TTL

The interface is designed for simple use with both MCU and bidirectional PC parallel port.

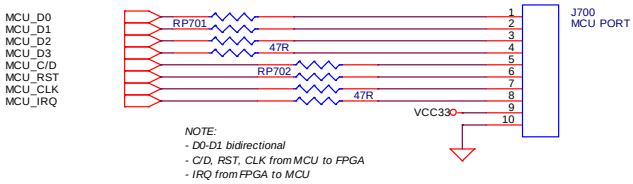

Fig.20: Microcontroller port

Protocol

Signal descriptions:

- **MCU_D0… MCU_D3** – 4 bit wide bidirectional data bus
- **MCU_C/D** – command or data selection, changing the level resets the cycle counter
- **MCU_RST** – global reset from MCU to FPGA
- **MCU_CLK** – clock signal, on edge writes the data to command/data registers
- **MCU_IRQ** – a feedback signal or event notification from FPGA to MCU

When transferring data, a command must be issued. If a command is a read command, the MCU must free the data bus during the stable phase of CLK signal, since on the next edge of CLK, the data will be outputted from FPGA.

Service components

JTAG port

This JTAG header is designed for easy use with the programmer from trenz-electronic.

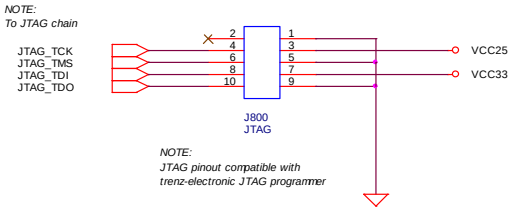

Fig.21: JTAG header

Reload button

The button is used to reload the image from PROM to FPGA. A need for reload which does also all the re-initialization may happen if the controller gets locked.

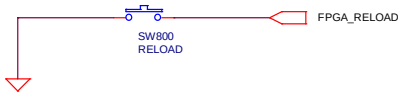

Fig.22: Reload pushbutton

Firmware structure

The internal structure of the FPGA in the controller contains the following blocks:

- **Ethernet interface** – reads frames from the Ethernet MAC
- **Packet filter** – which categorizes video data and DHCP/ARP, and also takes care of unwanted packets (act as a firewall)
- **RX/TX FIFOs** – for packets or frames
- **Video decoder** – which handles the network data and turns them into memory writes, the supported data formats might be:
    - uncompressed:
        - RGB
        - YUV
    - compressed:
        - RLE
        - JPEG
        - MPEG
- **WR/CMD/RD FIFOs** – part of the memory controller interface, the commands as well as the data in two directions are placed in these separate FIFOs
- **Synchronization signal generator** – generates HSync, VSync, DataEnable as well as memory read commands for prefetching the video data
- **Video output** – precisely outputs pixels in each clock cycle
- **MCU interface** – interfaces the FPGA with an MCU for DHCP/ARP handling as well as power management
- **On/Off registers** – for LVDS power, panel power and backlit unit on/off signals
- **LED control block** – is responsible for color coded information on the LEDs in the RJ45 connector

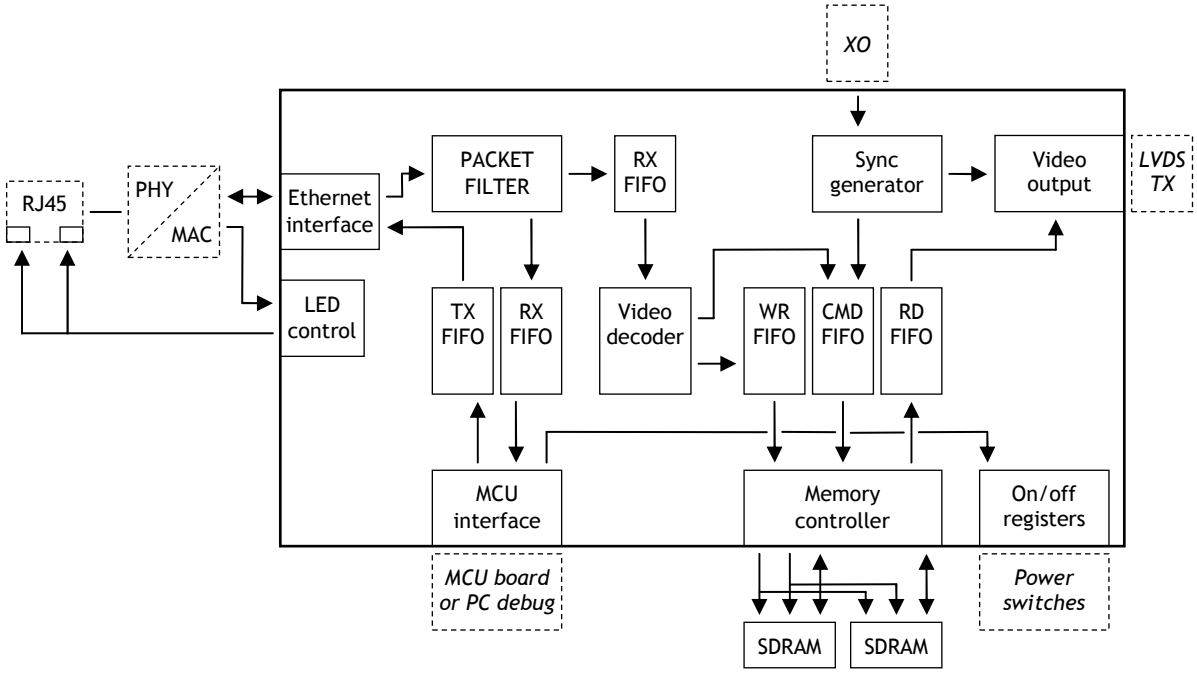

Fig.23: Internal structure of the FPGA for the display controller