

ETHERNET ATTACHED TFT DISPLAY CONTROLLER PROTOTYPE

SCHEMATIC DIAGRAMS

REVISION 0.5
FEBRUARY 2007

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Revision history

0.5 (2007-02-10)

- MCU, GPIO and CF changed to 5V variant, for higher frequency
- Bus separators placed between FPGA and MCU

0.4 (2007-02-09)

- MCU interface changed to 8 bits
- Onboard microcontroller - ATmega128
 - Brightness by digitally controlled resistance
 - Compact flash slot
 - Dual PS/2 ports
 - RS232 port
 - Unused pins: GPIO header, with dedicated regulated power supply
- Added an RGB TTL port
- Jumperless design - wired for usual configuration 3.3V/5V panel, 12V inverter
- Power supply for 1.2, 2.5, 3.3 and 5V included with 4 additional output headers
- Removed internal structure, document is schematics only

0.3 (2006-08-30)

- Added oscillator as a clock source for video controller

0.2 (2006-08-29)

- Added diagram of the internal structure of the controller - inside FPGA

0.1 (2006-08-28)

- Initial revision

Block diagram

External connections

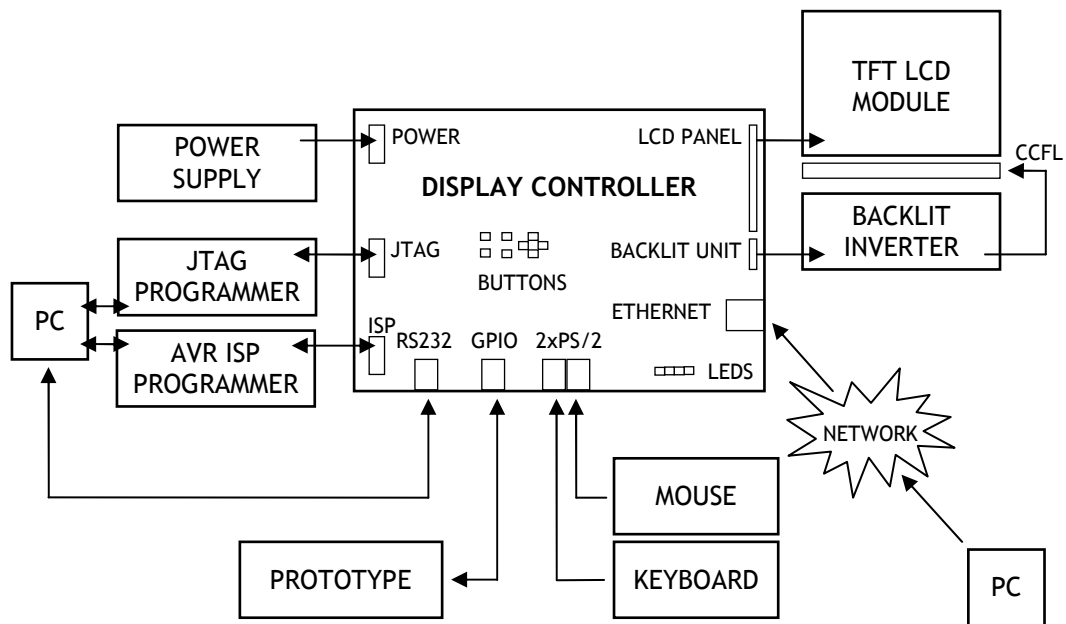


Fig.1: External connections to the display controller

List of connection points:

- *Power*
 - **Power input** [J110, J120] - source for 12V
 - **Power switch** [J130, J140] - an external power switch and internal jumper
 - **Power output** [J191...J194] - provides all main voltages to external devices
- *Programming ports*
 - **JTAG** [J200] - to program the FPGA
 - **AVR-ISP** [J300] - to program the MCU
- *Communication ports on MCU*
 - **PS/2** [J310, J320] - usually for keyboard and mouse
 - **RS232** [J330] - connection to a PC or the board could be used as a console
 - **GPIO** [J340] - general purpose, 18 bidirectional lines from MCU
- *Communication ports on FPGA*
 - **Ethernet** [J400] - 10/100 Mbps, with full duplex capability, AUTO MDI-X
- *LCD panel outputs*
 - **RGB TTL** [J510] type - parallel connection for low resolutions
 - **LVDS** [J530] type - serial connection for high resolutions
- *Memory card*
 - **Compact Flash** [J600] - CF card interface (operates in 8bit IDE mode)

Detailed schematics

Power supplies

The power supply is composed of several separate switched mode power supplies. While the first one is a dual output SMPS with MAX1634, the two lower voltage stages are powered from 5V and use the MAX1714B controller. The auxiliary regulated power supply is realized with MC34063.

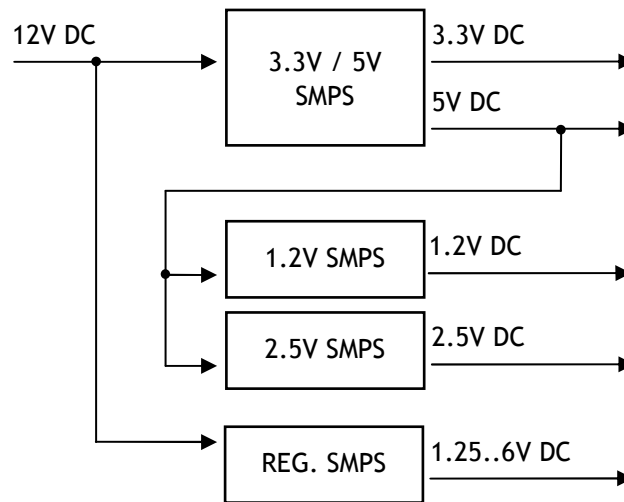


Fig.3: Block diagram of the power supplies

The usage of voltages is the following:

- Unstabilized
 - 12V - backlit power
- Stabilized
 - 1.2V - FPGA core
 - 2.5V - JTAG chain
 - 3.3V - FPGA input/output, Ethernet, memory, LVDS, TFT panel power
 - 5.0V - backlit on/off control, brightness range, optional TFT panel power, MCU, Compact Flash, PS/2, RS232, GPIO

Power input and switching

The input connectors are PC-style power connectors. Both 5.25" (J110) and 3.5" (J120) power connectors are present on the board. The board itself uses only the 12V input line even if there is a 5V line. After the input, the power is switched through an external switch (J130) or could be set to always on using a jumper (J140).

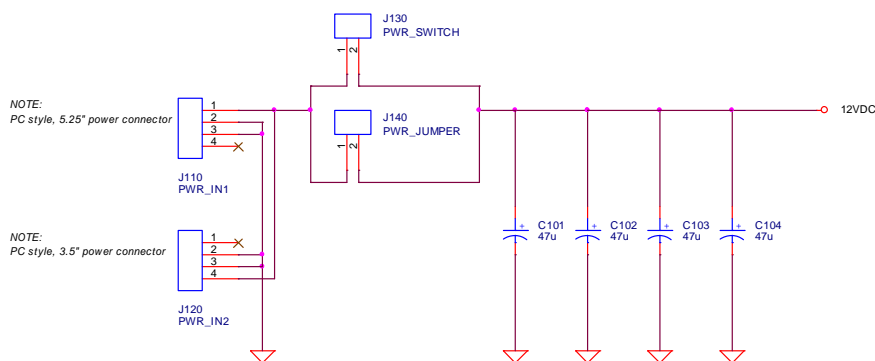


Fig.4: Input connectors and input power switching

3.3V/5.0V dual power supply

The 5V output line is used only for the brightness adjustment and backlit on/off control. Because these represent no heavy load, it is also used for powering the lower voltage supplies (1.2V and 2.5V).

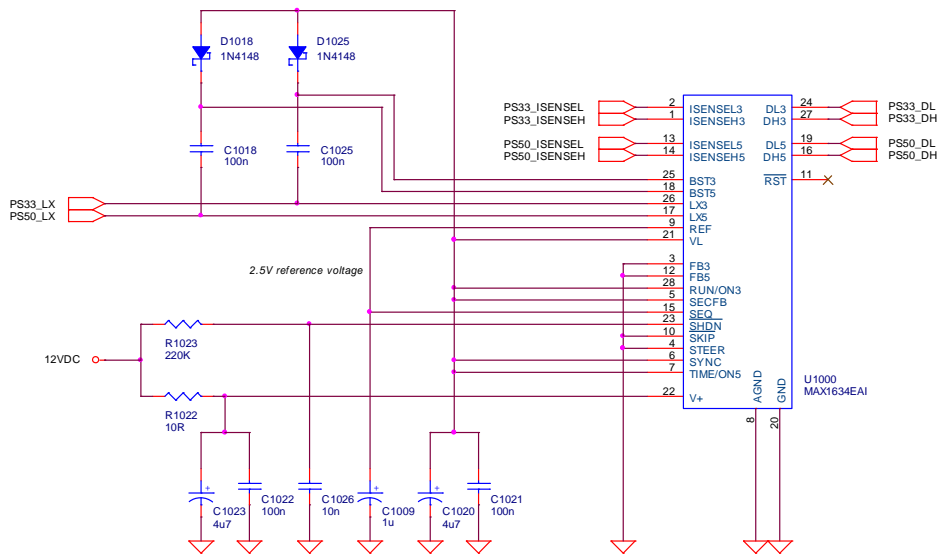


Fig.5: The 3.3V and 5.0V switched mode dual power supply controller

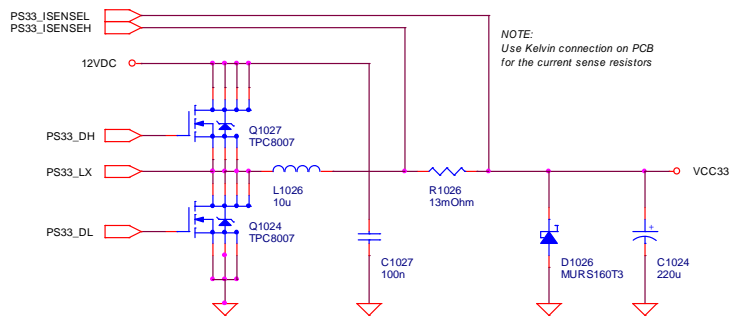


Fig.6: The 3.3V output stage

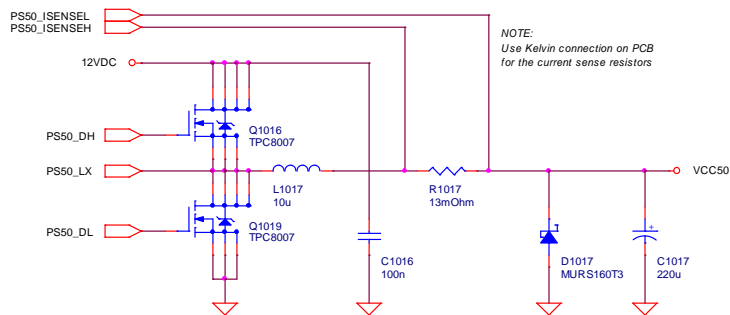


Fig.7: The 5.0V output stage



Fig.8: Power on indicators

1.2V power supply

Uses a MAX1714B controller which is configured with two external resistors for 1.2V:

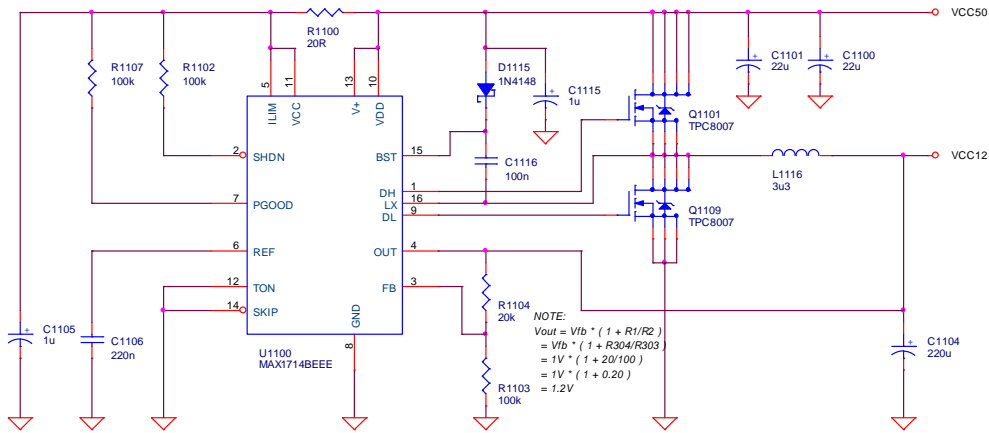


Fig.9: The 1.2V switched mode power supply

2.5V power supply

Uses a MAX1714B controller which is configured internally for 2.5V (FB grounded):

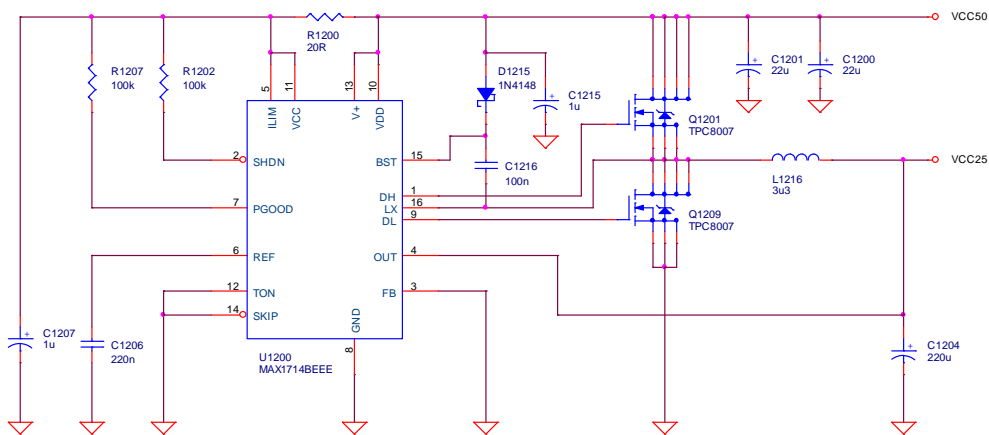


Fig.10: The 2.5V switched mode power supply

Regulated auxiliary power supply

Output of this power supply is used only on the GPIO port so it is dedicated for powering various prototypes and/or components under reverse engineering or development. The circuit is based on an MC34063 regulator, the output can be set from 1.25V to 5.87V (limit defined by R1352).

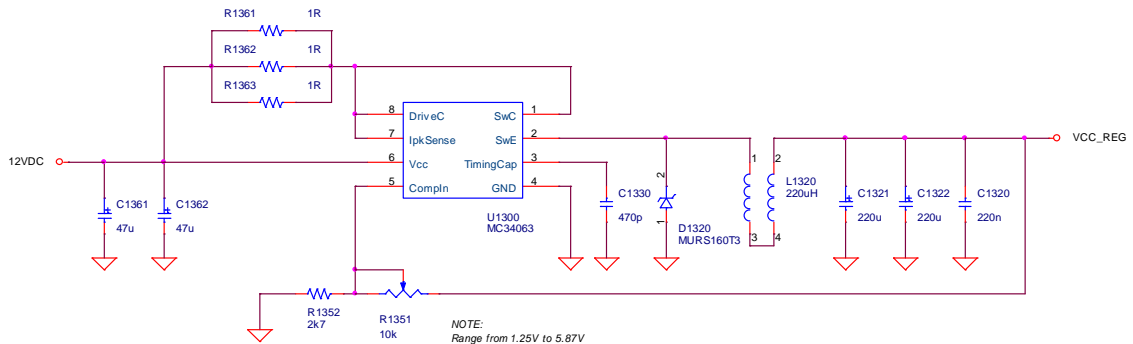


Fig.11: The regulated auxiliary switched mode power supply

Additional power output connectors

Four additional headers with 1.2V, 2.5V, 3.3V, 5.0V and 12V voltages are available to power external equipment or additional development boards.

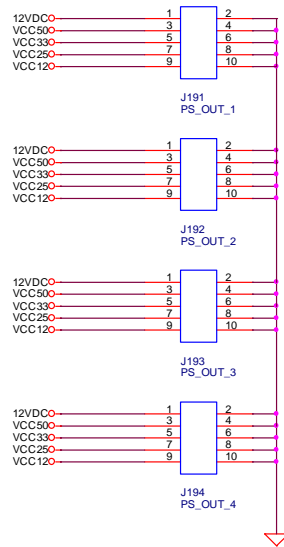


Fig.12: The additional power output connectors

FPGA

The largest low cost FPGA (in non-BGA package) from Xilinx is used, which is currently the Spartan 3E with 500K equivalent gates (part number: XC3S500E-PQ208).

Power

JTAG chain is powered by $V_{CCAUX} = 2.5V$ and the internals (core) runs with $V_{CCINT} = 1.2V$. All four input/output banks are configured with $V_{CC0} = 3.3V$. A decoupling capacitor is placed next to each power input pin.

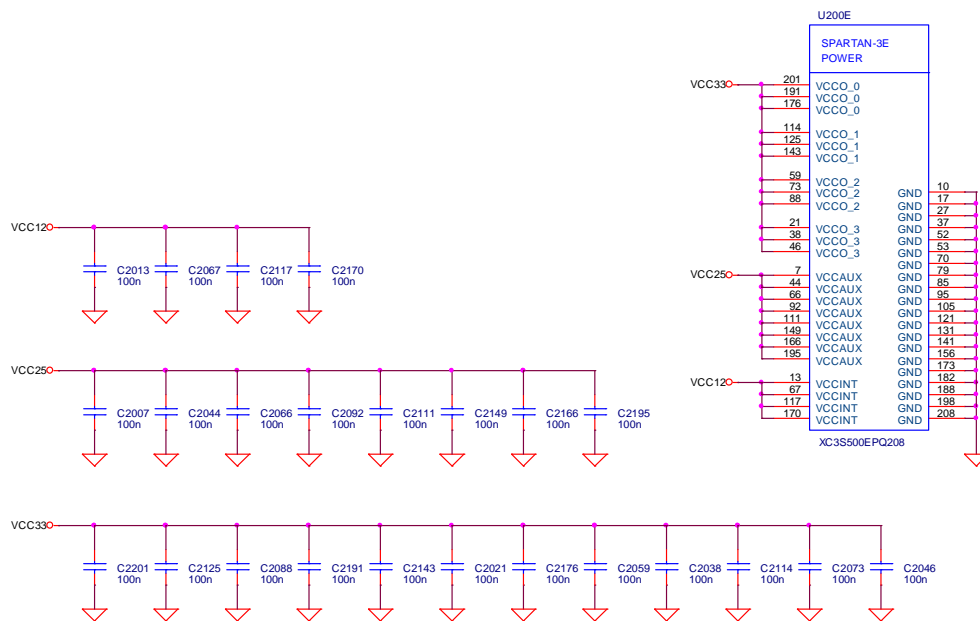


Fig.13: FPGA power distribution

Configuration PROM

The configuration is stored in a Xilinx Platform Flash. Its inputs and outputs run on $V_{CC0} = 3.3V$.

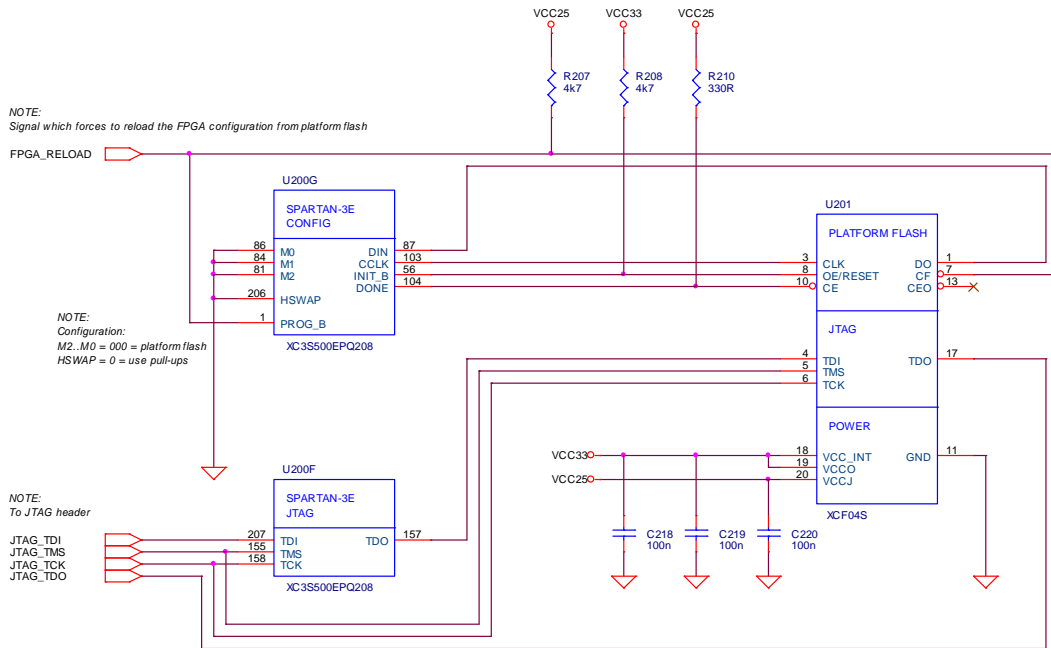


Fig.14: FPGA configuration PROM and JTAG chain

Input output pin assignment

The preliminary distribution of input/output pins (the exact assignment of pins can change with the PCB design phase):

- Memory: top and right edge
- Ethernet: left edge
- Display data (to RGB port and LVDS transmitter): bottom edge
- Microcontroller: top-left corner

There are several unused input pins.

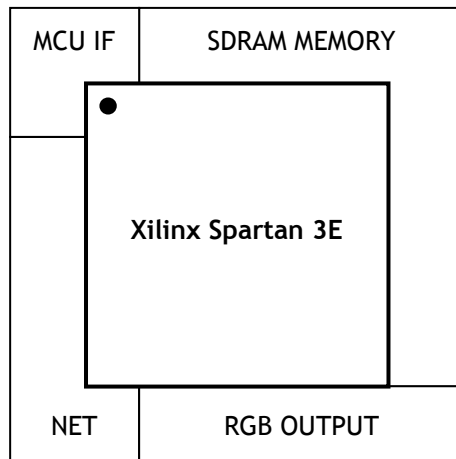


Fig.15: FPGA pin assignment - block diagram

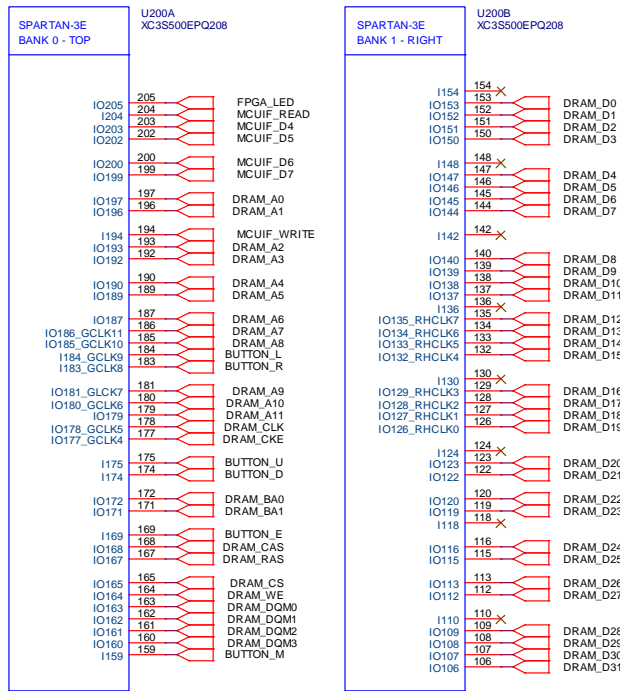


Fig.16: Top and right edge

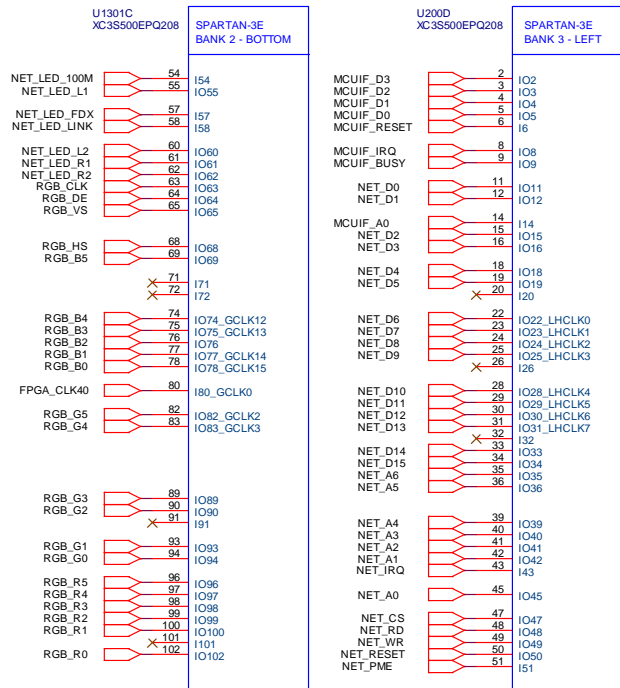


Fig.17: Bottom and left edge

Configuration Reload button

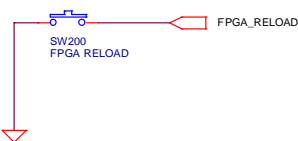


Fig.18: FPGA reload configuration button

Additional FPGA keypad

The 4 buttons represent the directions (*up/down/left/right*) and the other two are the *menu* and *escape* buttons. The keypad could be used for a simple OSD.

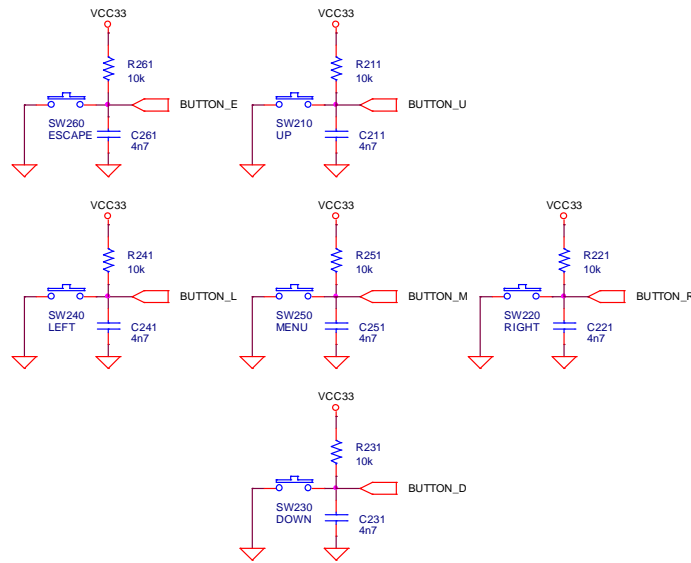


Fig.19: FPGA keypad

Clock source

A precise clock source is made from a crystal oscillator. The frequency is 40MHz which allows us to generate both 65 MHz (XGA) and 85MHz (WXGA) pixel clock using a single DCM inside the FPGA. The SDRAM clock (133 MHz) can be achieved by the same way.

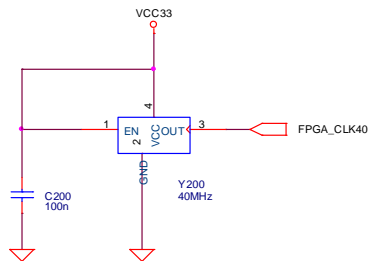


Fig.20: Clock source

FPGA LED

This is a general purpose indicator.

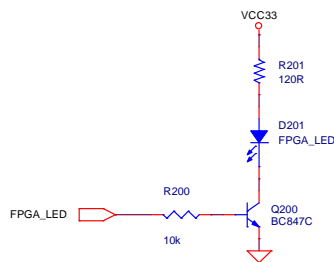


Fig.21: FPGA LED

Microcontroller unit

MCU core

Contains the ATmega128 microcontroller clocked to 16MHz (component maximum). Because the interface with FPGA is on 3.3V, there are two bus separators which has 5V tolerant pins on their B side.

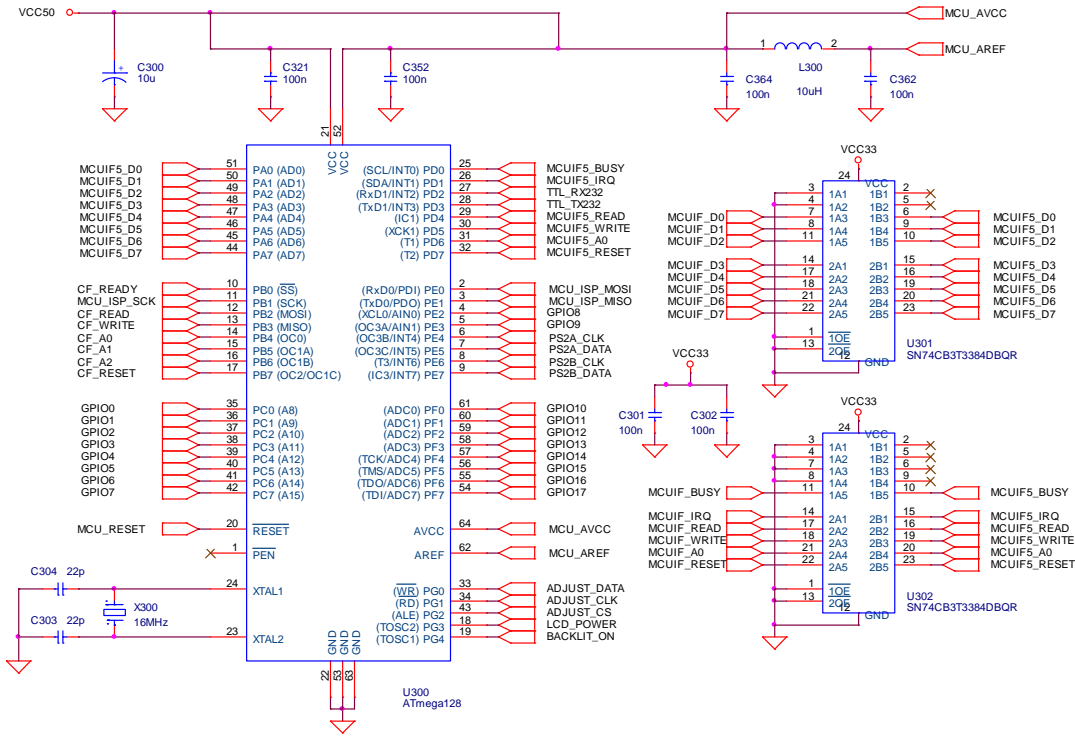


Fig.22: MCU core system

PS/2 ports

The dual PS/2 ports are operating at 5V. Usually used for keyboard and mouse.

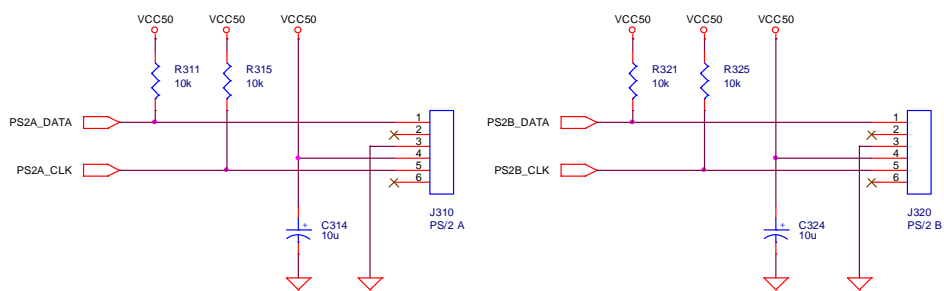


Fig.23: Dual PS/2 ports

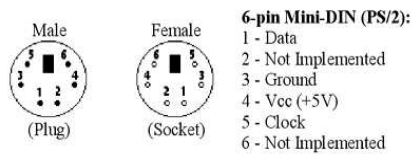


Fig.24: Pinout of the PS/2 connector

Ethernet

The LAN9218I integrated PHY/MAC is connected to FPGA using a 16 bit bus and uses an external EEPROM chip to store its physical network address (MAC address).

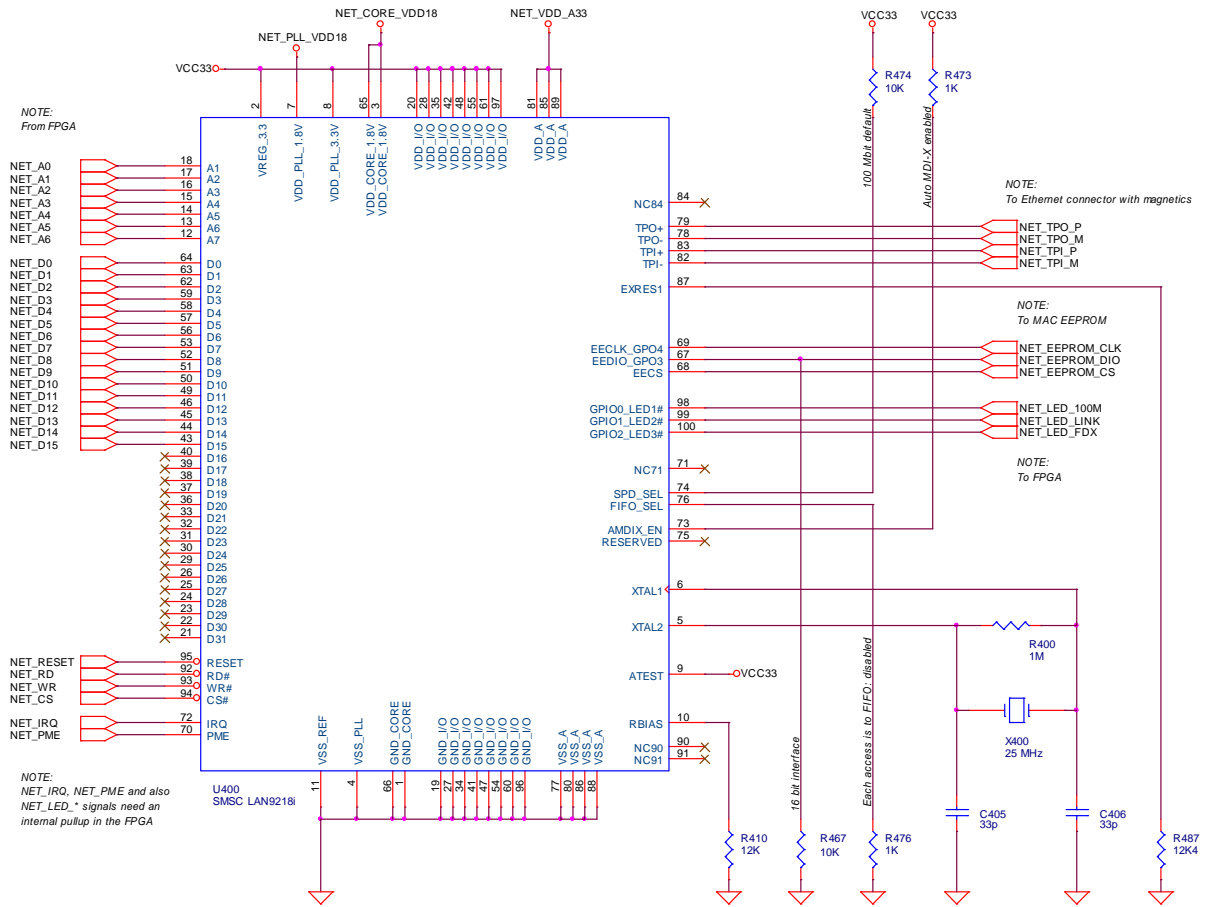


Fig.28: Integrated PHY/MAC with configuration setup

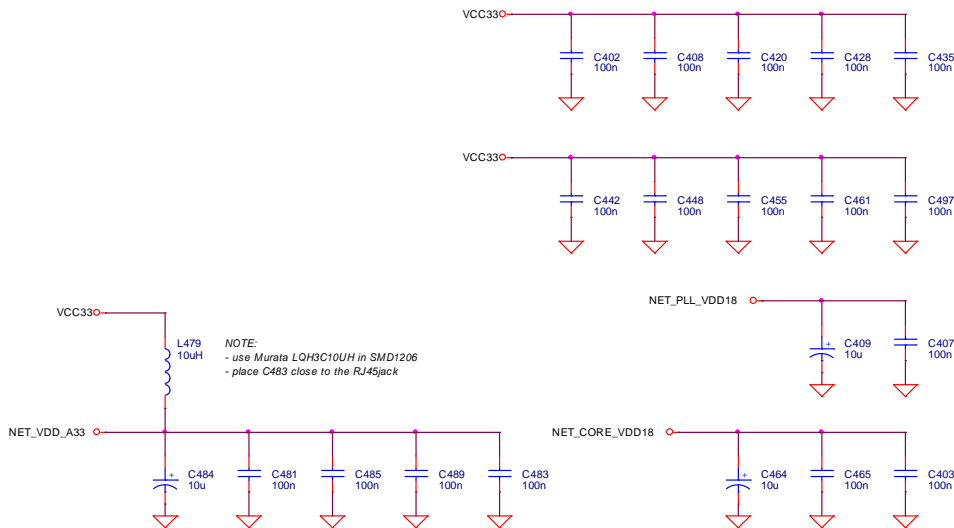


Fig.29: Network controller decoupling capacitors

Backlit on/off indicator

Controlled by the MCU.

Backlit on/off signal is created fully by the MCU.

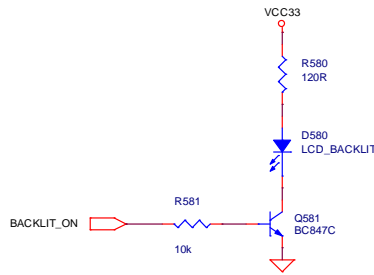


Fig.33: Backlit on/off indicator

Backlit brightness adjustment

Controlled by the MCU.

Digitally controlled resistance is used to control the brightness of the CCFL.

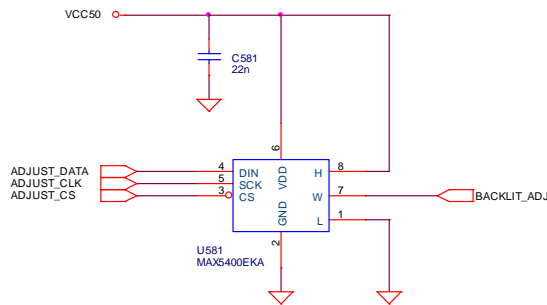


Fig.34: Digitally controlled resistor for brightness adjustment

LVDS transmitter

This transmitter converts the parallel (TTL RGB) input to serial (LVDS) output.

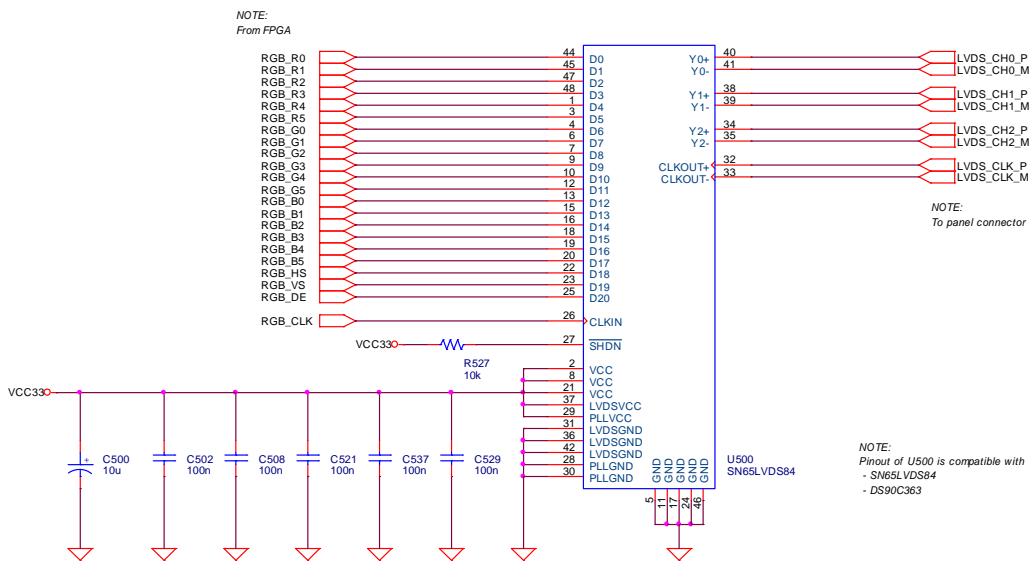


Fig.35: An 18-bit LVDS transmitter with decoupling capacitors

LCD panel ports

The output headers provides both 3.3V and 5V for use as the LCD panel power thus the selection of the proper voltage is made by proper wiring of the cable from the controller board to the LCD panel.

RGB TTL type

Uses a 40 pin header (2x20 pins)

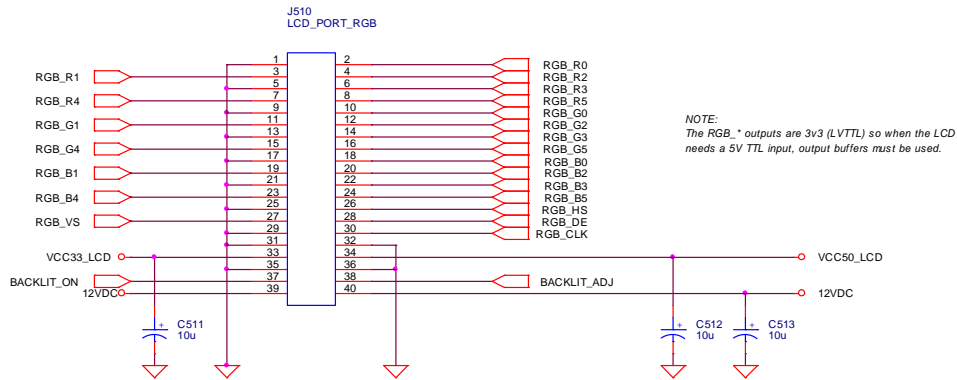


Fig.36: Connector for RGB TTL panels

LVDS type

Uses a 34 pin header (2x17 pins)

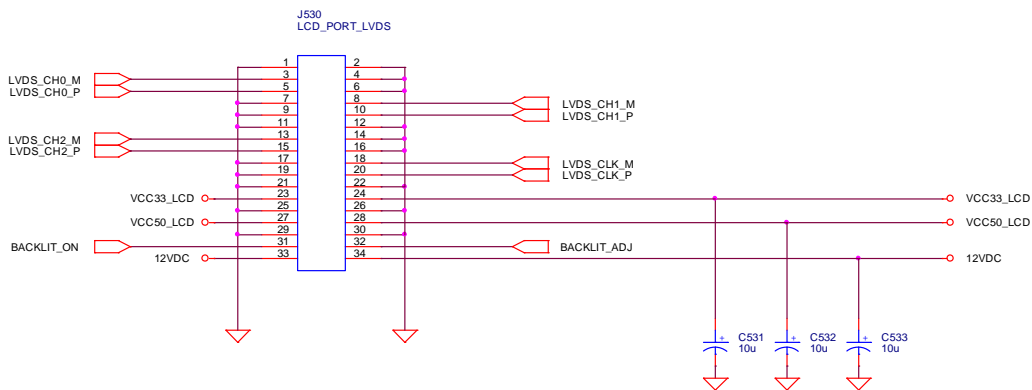


Fig.37: Connector for LVDS panels

Memory card

There is a CF card socket which is wired to operate in a true IDE mode at 8bit. The data bus is shared with the MCU-FPGA interface so that the data exchange can save a cycle on each byte.

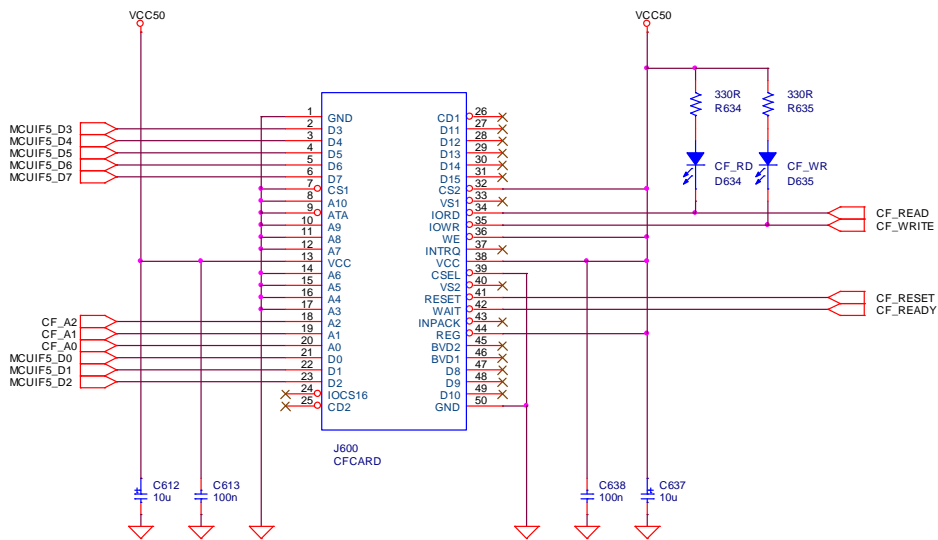


Fig.38: Compact flash socket

Main memory

There is 16MB memory on the board which is made from 2 chips - for wider data path (2x16=32bit). When operating at 133MHz, the peak transfer rate of the memory system is 533MB/s.

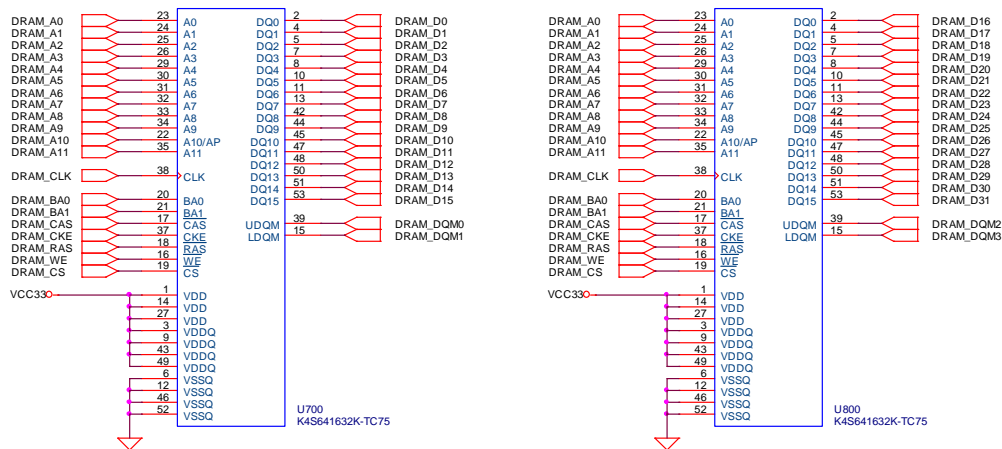


Fig.39: The two memory chips

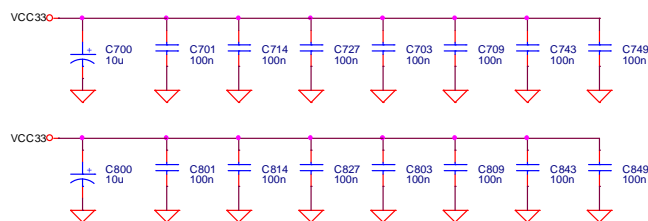


Fig.40: Decoupling capacitors for each power pin of memory

Programming

JTAG for FPGA

This JTAG header is designed for easy use with the programmer from trenz-electronic.

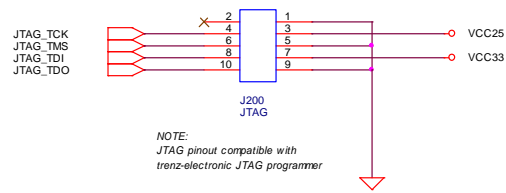


Fig.41: JTAG header

AVRISP for MCU

This AVRISP header is designed for use with the original AVRISP programmer from Atmel.

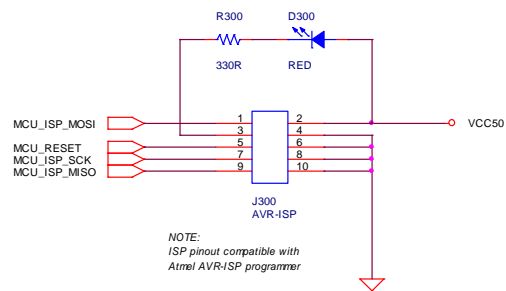


Fig.42: AVR ISP header

Reset button for MCU

This button restarts the microcontroller and the RC circuit provides also the power-on reset.

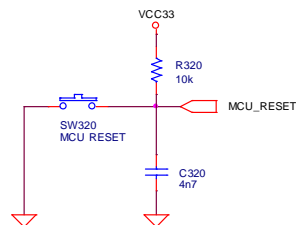


Fig.43: MCU reset button