

# ETHERNET ATTACHED TFT DISPLAY CONTROLLER

PROTOTYPE SCHEMATIC DIAGRAMS

REVISION 0.6  
FEBRUARY 2007

- Revision history .....3
- Block diagram .....4
  - External connections .....4
  - Internal structure .....5
- Detailed schematics .....6
  - Power supplies.....6
    - Power input and switching .....6
    - 3.3V/5.0V dual power supply .....7
    - 1.2V power supply .....8
    - 2.5V power supply .....8
    - Regulated auxiliary power supply .....8
    - Additional power output connectors .....9
  - FPGA.....9
    - Power.....9
    - Configuration PROM..... 10
    - Input output pin assignment ..... 10
    - Additional FPGA keypad..... 12
    - Clock source..... 12
    - FPGA LED ..... 12
  - Microcontroller unit ..... 13
    - MCU core..... 13
    - PS/2 ports ..... 13
    - RS232 serial port ..... 14
    - General purpose inputs/outputs - GPIO headers ..... 14
  - Ethernet ..... 15
  - Display module ..... 16
    - Power switching ..... 16
    - Backlit on/off indicator ..... 17
    - Backlit brightness adjustment ..... 17
    - LVDS transmitter ..... 17
    - LCD panel ports..... 18
      - RGB TTL type..... 18
      - LVDS type ..... 18
  - Memory card ..... 19
  - Main memory ..... 19
  - I2S bus ..... 20

I2S audio decoder .....	20
I2S data decoder .....	20
Data decoder.....	20
General purpose LED's .....	21
General purpose outputs - GPO headers .....	21
Programming.....	22
JTAG for FPGA .....	22
AVRISP for MCU .....	22
Initialization .....	22
Configuration Reload button .....	22
Reset button for MCU.....	22

## Revision history

### 0.6 (2007-02-11)

- Audio output using I2S DAC
- I2S data decoder - 32bits of GPO
  - RJ45 LEDs connected here
  - 4 new general purpose LEDs
  - 24 bit GPO on 3 headers per 8bits

### 0.5 (2007-02-10)

- MCU, GPIO and CF changed to 5V variant, for higher frequency
- Bus separators placed between FPGA and MCU

### 0.4 (2007-02-09)

- MCU interface changed to 8 bits
- Onboard microcontroller - ATmega128
  - Brightness by digitally controlled resistance
  - Compact flash slot
  - Dual PS/2 ports
  - RS232 port
  - Unused pins: GPIO header, with dedicated regulated power supply
- Added an RGB TTL port
- Jumperless design - wired for usual configuration 3.3V/5V panel, 12V inverter
- Power supply for 1.2, 2.5, 3.3 and 5V included with 4 additional output headers
- Removed internal structure, document is schematics only

### 0.3 (2006-08-30)

- Added oscillator as a clock source for video controller

### 0.2 (2006-08-29)

- Added diagram of the internal structure of the controller - inside FPGA

### 0.1 (2006-08-28)

- Initial revision

## Block diagram

### External connections

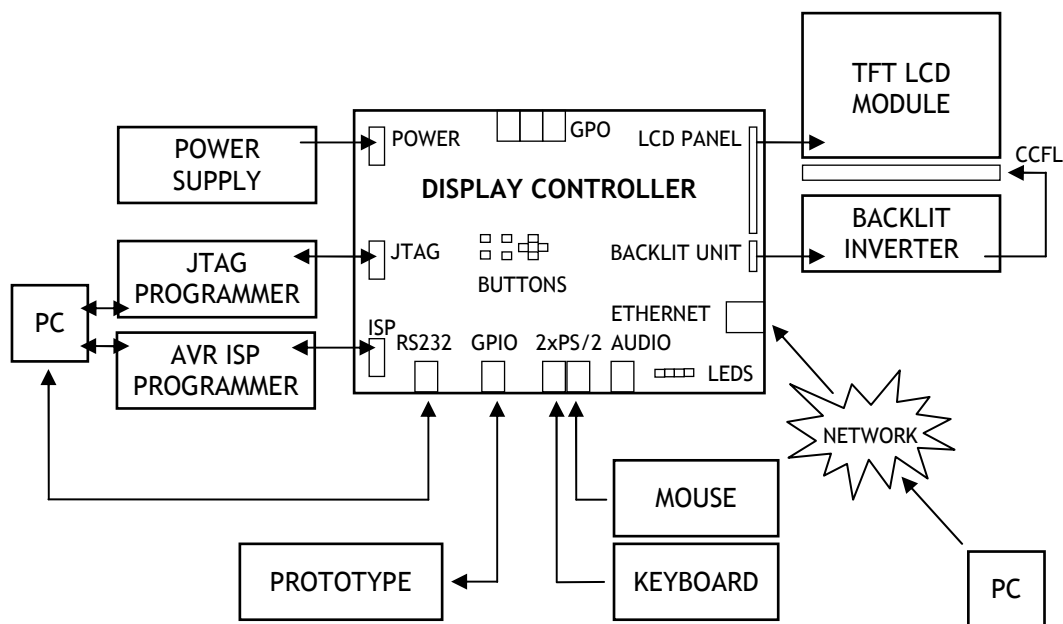


Fig.1: External connections to the display controller

List of connection points:

- *Power*
  - **Power input** [J110, J120] - source for 12V
  - **Power switch** [J130, JP140] - an external power switch and internal jumper
  - **Voltmeter** [J150] - indicator for the AUX power supply
  - **Power output** [J191...J194] - provides all main voltages to external devices
- *Programming ports*
  - **JTAG** [J200] - to program the FPGA
  - **AVR-ISP** [J300] - to program the MCU
- *Communication ports on MCU*
  - **PS/2** [J310, J320] - usually for keyboard and mouse
  - **RS232** [J330] - connection to a PC or the board could be used as a console
  - **GPIO** [J340, J341, J342] - general purpose, 18 bidirectional lines from MCU
- *Communication ports on FPGA*
  - **Ethernet** [J400] - 10/100 Mbps, with full duplex capability, AUTO MDI-X
- *LCD panel outputs*
  - **RGB TTL** [J510] type - parallel connection for low resolutions
  - **LVDS** [J530] type - serial connection for high resolutions
- *Memory card*
  - **Compact Flash** [J600] - CF card interface (operates in 8bit IDE mode)
- *Outputs decoded from I2S*
  - **GPO** [J901, J902, J903] - 24 bits output (8 per header), synced with audio
  - **Audio output** [J990, J991, J992] - from a stereo 16 bit DAC

## Internal structure

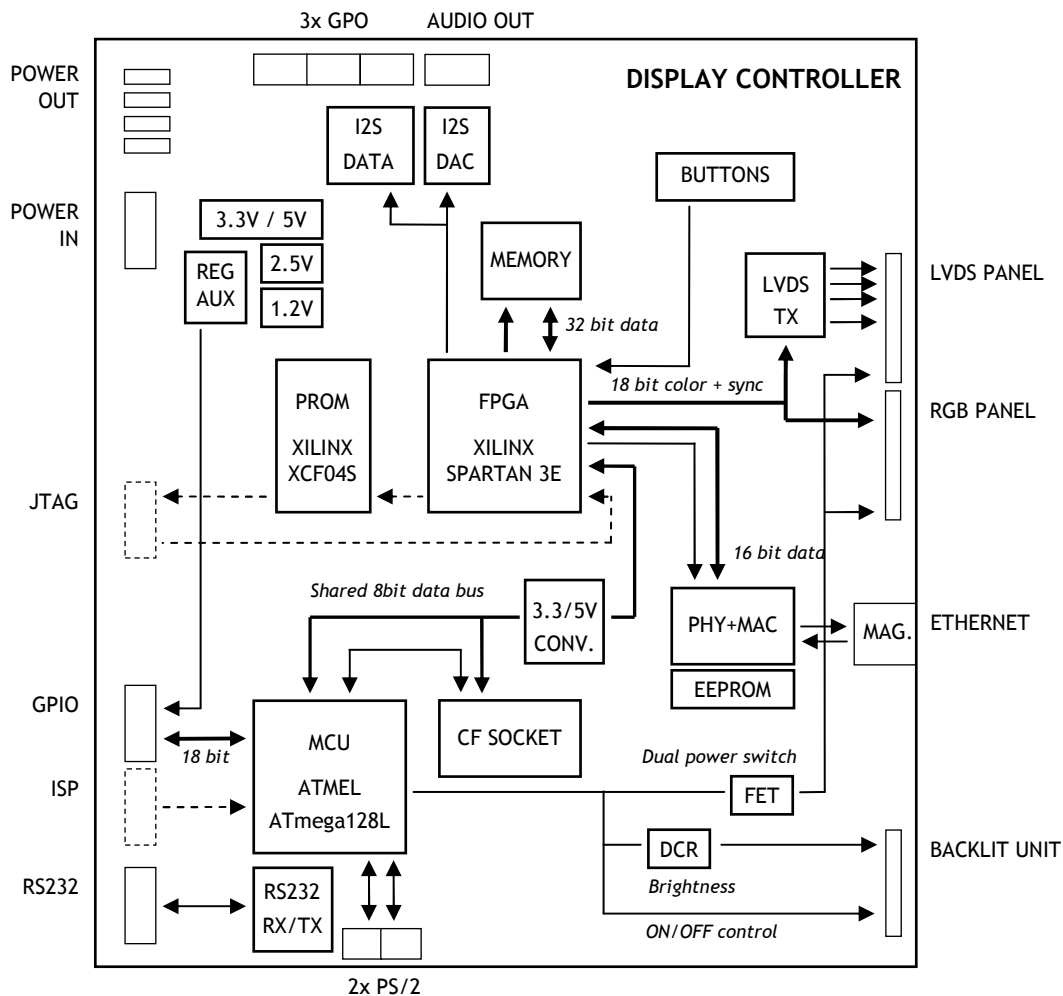


Fig.2: Internal structure of the display controller

### Buttons:

- FPGA reload [SW200]
- MCU reset [SW320]
- 6 user keys (4 directional and enter/escape) [SW210, SW220, ... SW260]

### Indicators:

- Power: 3.3V [D133], 5.0V [D150]
- FPGA LED [D201]
- AVR ISP connected [D300]
- RS232: RX [D332], TX [D333]
- Backlit on [D580]
- LCD power on [D590]
- Compact Flash card Read: [D634], Write [D635]
- 4 GPO LEDs on I2S [D906, D907, D908, D909]
- Additionally, the RJ45 ethernet port has two dual color LEDs (green/orange)

## Detailed schematics

### Power supplies

The power supply is composed of several separate switched mode power supplies. While the first one is a dual output SMPS with MAX1634, the two lower voltage stages are powered from 5V and use the MAX1714B controller. The auxiliary regulated power supply is realized with MC34063.

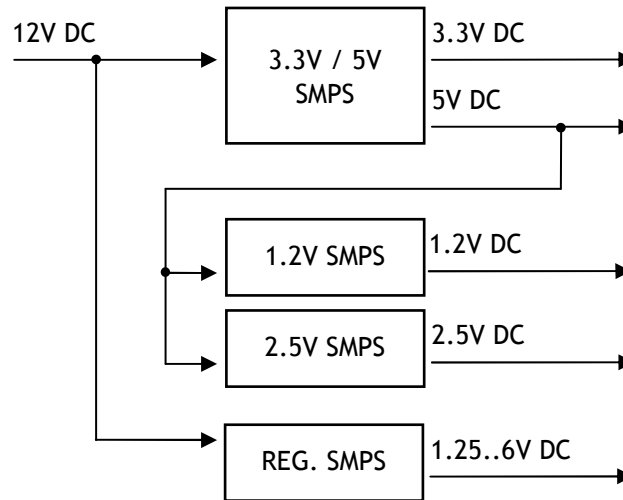


Fig.3: Block diagram of the power supplies

The usage of voltages is the following:

- Unstabilized
  - 12V - backlit power
- Stabilized
  - 1.2V - FPGA core
  - 2.5V - JTAG chain
  - 3.3V - FPGA input/output, Ethernet, memory, LVDS, TFT panel power
  - 5.0V - backlit on/off control, brightness range, optional TFT panel power, MCU, Compact Flash, PS/2, RS232, GPIO

### Power input and switching

The input connectors are PC-style power connectors. Both 5.25" (J110) and 3.5" (J120) power connectors are present on the board. The board itself uses only the 12V input line even if there is a 5V line. After the input, the power is switched through an external switch (J130) or could be set to always on using a jumper (JP140).

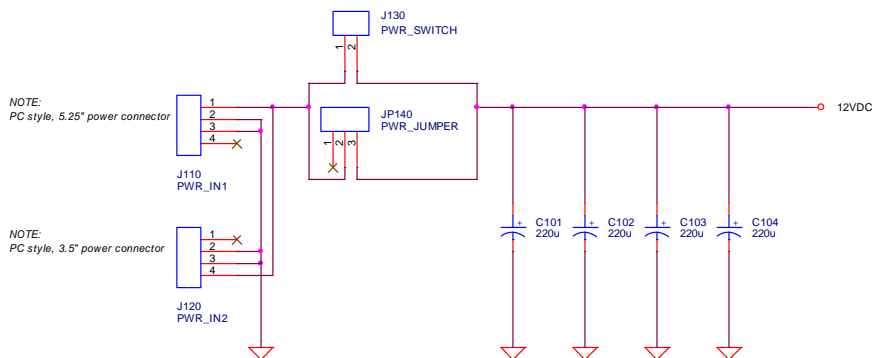


Fig.4: Input connectors and input power switching

### 3.3V/5.0V dual power supply

The 5V output line is used only for the brightness adjustment and backlit on/off control. Because these represent no heavy load, it is also used for powering the lower voltage supplies (1.2V and 2.5V).

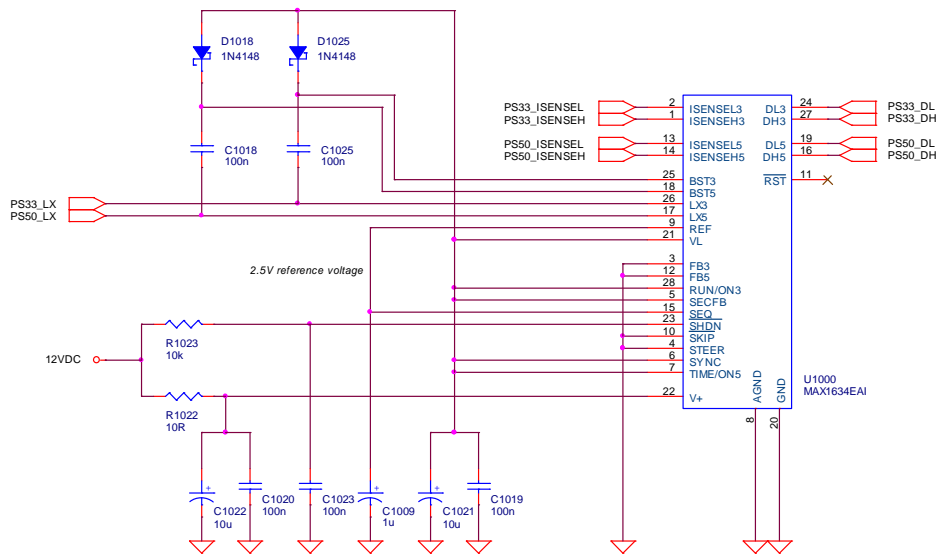


Fig.5: The 3.3V and 5.0V switched mode dual power supply controller

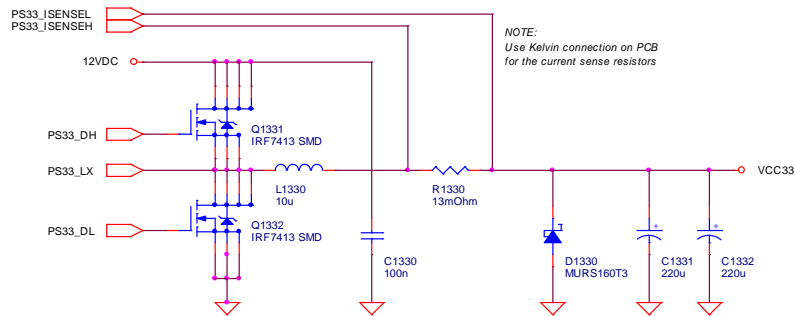


Fig.6: The 3.3V output stage

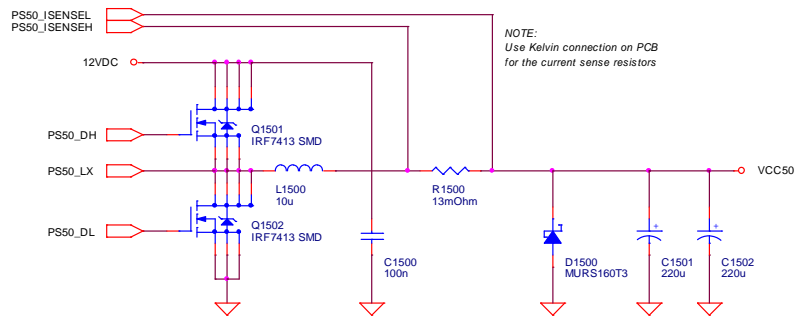


Fig.7: The 5.0V output stage



Fig.8: Power on indicators

### 1.2V power supply

Uses a MAX1714B controller which is configured with two external resistors for 1.2V:

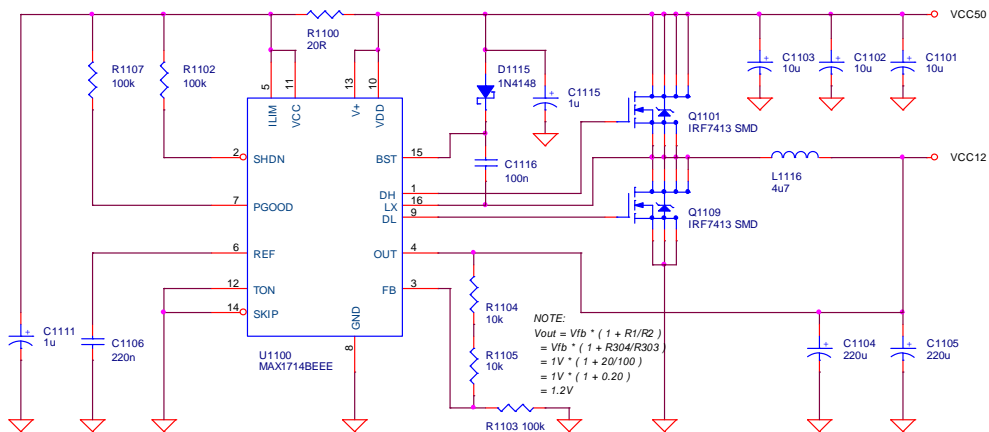


Fig.9: The 1.2V switched mode power supply

### 2.5V power supply

Uses a MAX1714B controller which is configured internally for 2.5V (FB grounded):

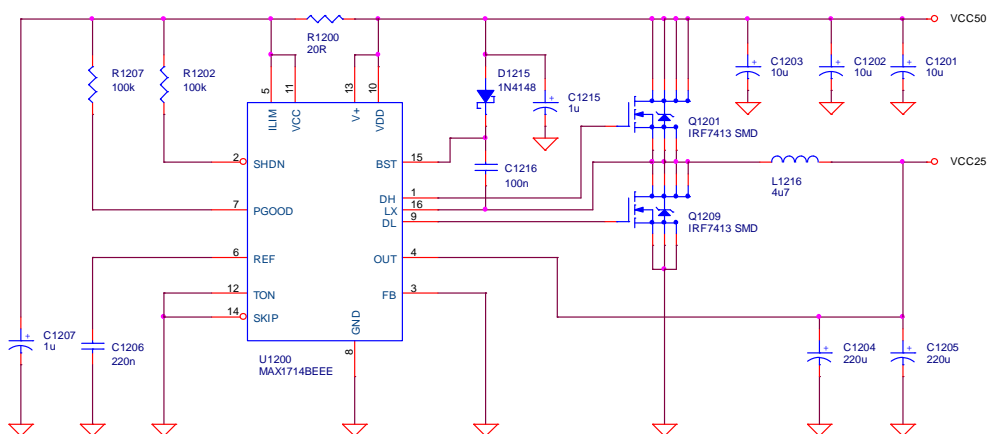


Fig.10: The 2.5V switched mode power supply

### Regulated auxiliary power supply

Output of this power supply is used only on the GPIO port. The circuit is based on an MC34063 regulator, the output can be set from 1.25V to 3.90V (limit defined by R1352). If the jumper JP1352 is present on 2-3, the maximal voltage is not limited to 3.90V.

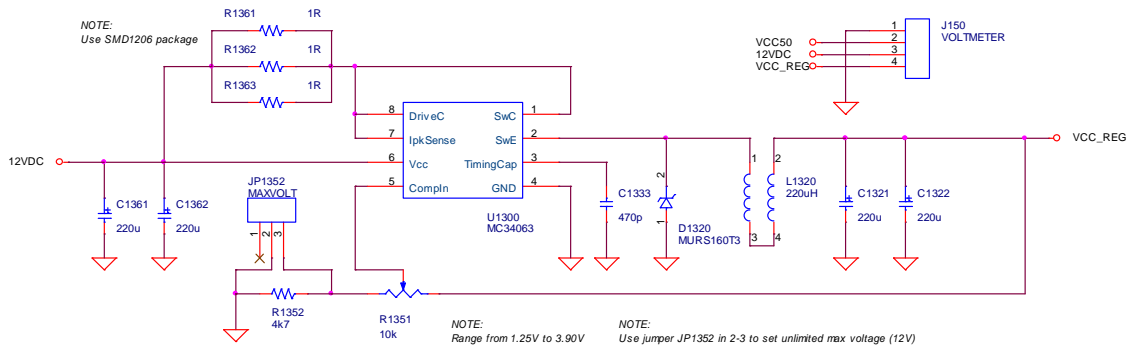


Fig.11: The regulated auxiliary switched mode power supply

### Additional power output connectors

Four additional headers with 1.2V, 2.5V, 3.3V, 5.0V and 12V voltages are available to power external equipment or additional development boards.

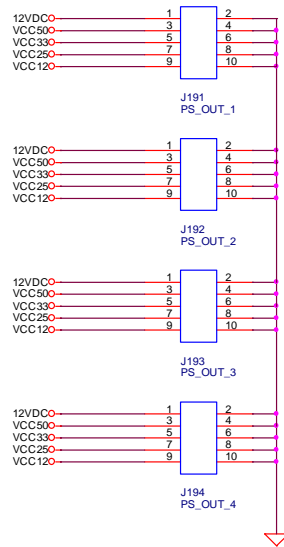


Fig.12: The additional power output connectors

### FPGA

The largest low cost FPGA (in non-BGA package) from Xilinx is used, which is currently the Spartan 3E with 500K equivalent gates (part number: XC3S500E-PQ208).

### Power

JTAG chain is powered by  $V_{CCAUX} = 2.5V$  and the internals (core) runs with  $V_{CCINT} = 1.2V$ . All four input/output banks are configured with  $V_{CCO} = 3.3V$ . A decoupling capacitor is placed next to each power input pin.

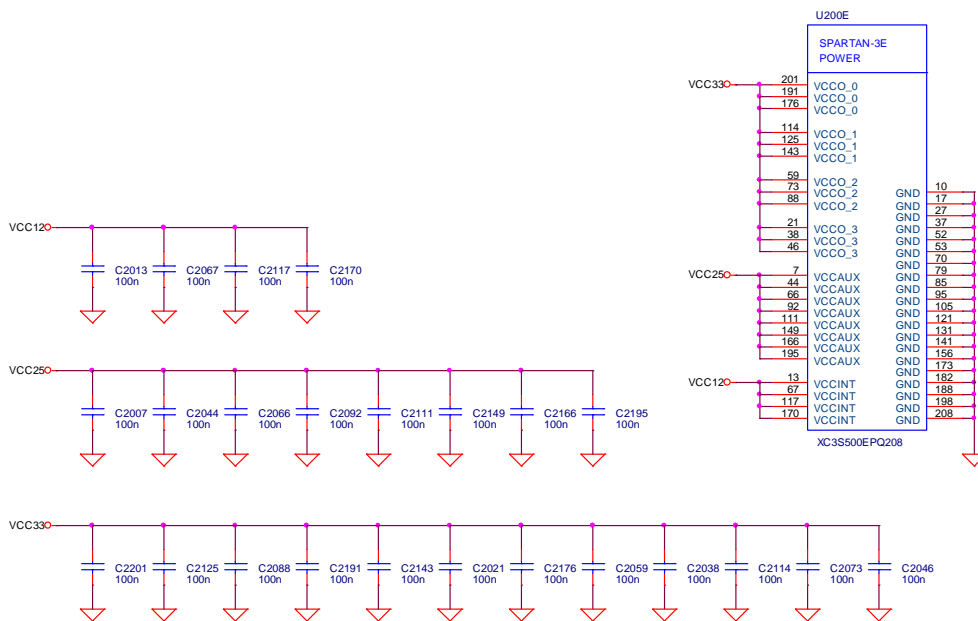


Fig.13: FPGA power distribution

### Configuration PROM

The configuration is stored in a Xilinx Platform Flash. Its inputs and outputs run on  $V_{CC0} = 3.3V$ .

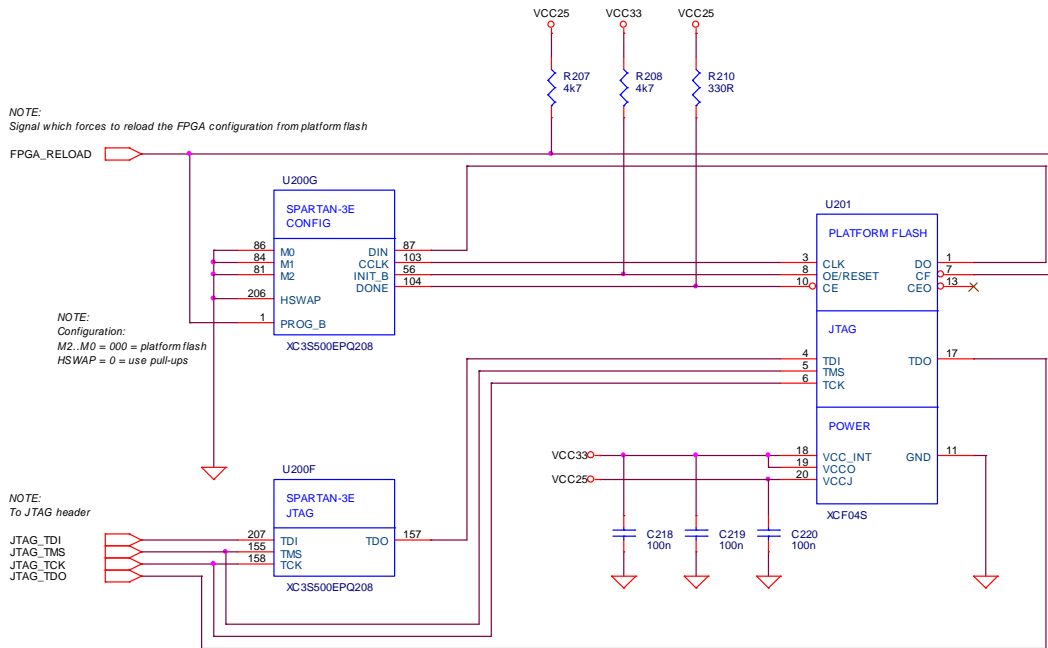


Fig.14: FPGA configuration PROM and JTAG chain

### Input output pin assignment

The preliminary distribution of input/output pins (the exact assignment of pins can change with the PCB design phase):

- Memory: top and right edge
- Ethernet: left edge
- Display data (to RGB port and LVDS transmitter): bottom edge
- Microcontroller: top-left corner

There are several unused input pins.

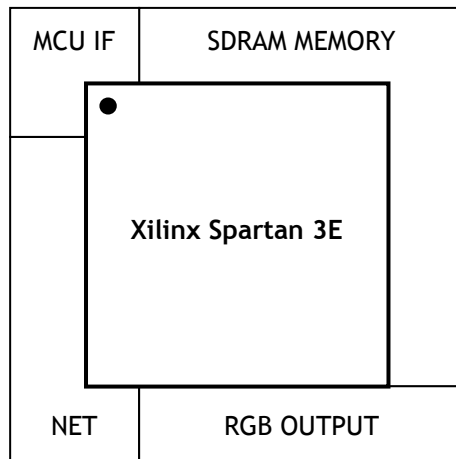


Fig.15: FPGA pin assignment - block diagram

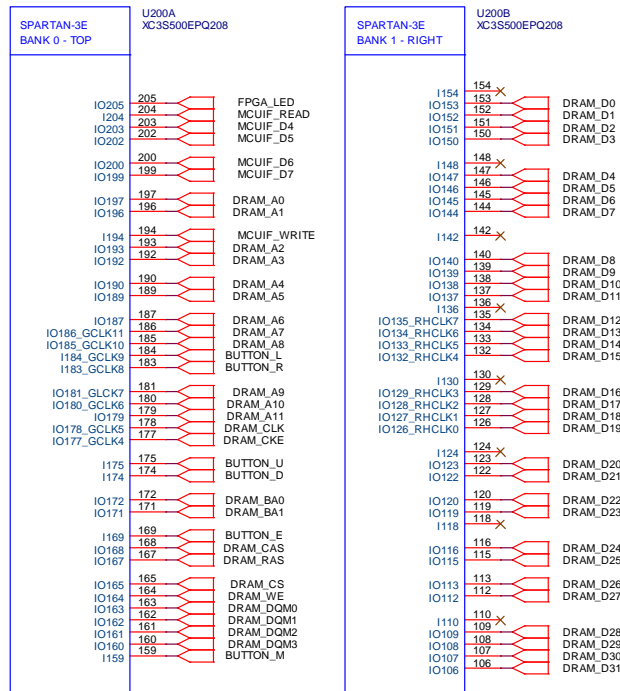


Fig.16: Top and right edge

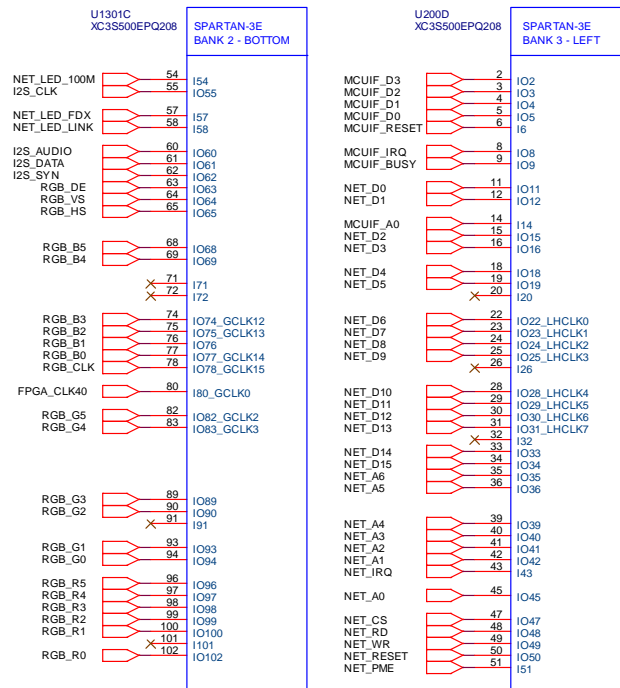


Fig.17: Bottom and left edge

### Additional FPGA keypad

The 4 buttons represent the directions (*up/down/left/right*) and the other two are the *menu* and *escape* buttons. The keypad could be used for a simple OSD.

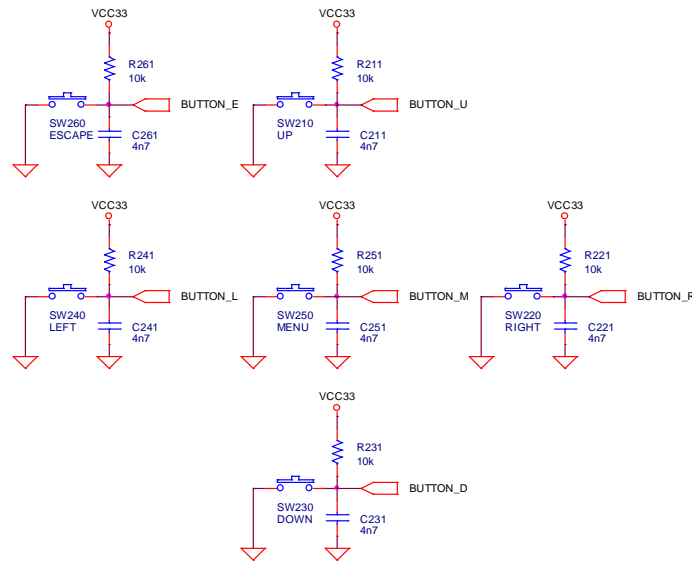


Fig.18: FPGA keypad

### Clock source

A precise clock source is made from a crystal oscillator. The frequency is 40MHz which allows us to generate both 65 MHz (XGA) and 85MHz (WXGA) pixel clock using a single DCM inside the FPGA. The SDRAM clock (133 MHz) can be achieved by the same way.

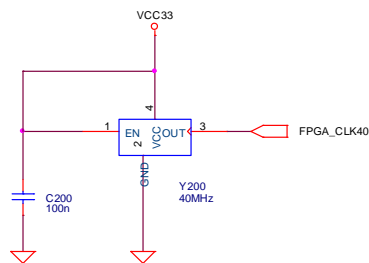


Fig.19: Clock source

### FPGA LED

This is a general purpose indicator.

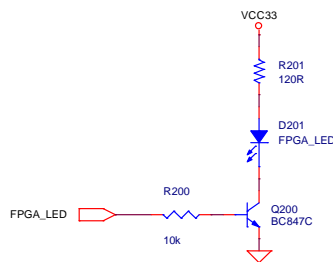


Fig.20: FPGA LED

# Microcontroller unit

## MCU core

Contains the ATmega128 microcontroller clocked to 16MHz (component maximum). Because the interface with FPGA is on 3.3V, there are two bus separators which has 5V tolerant pins on their B side.

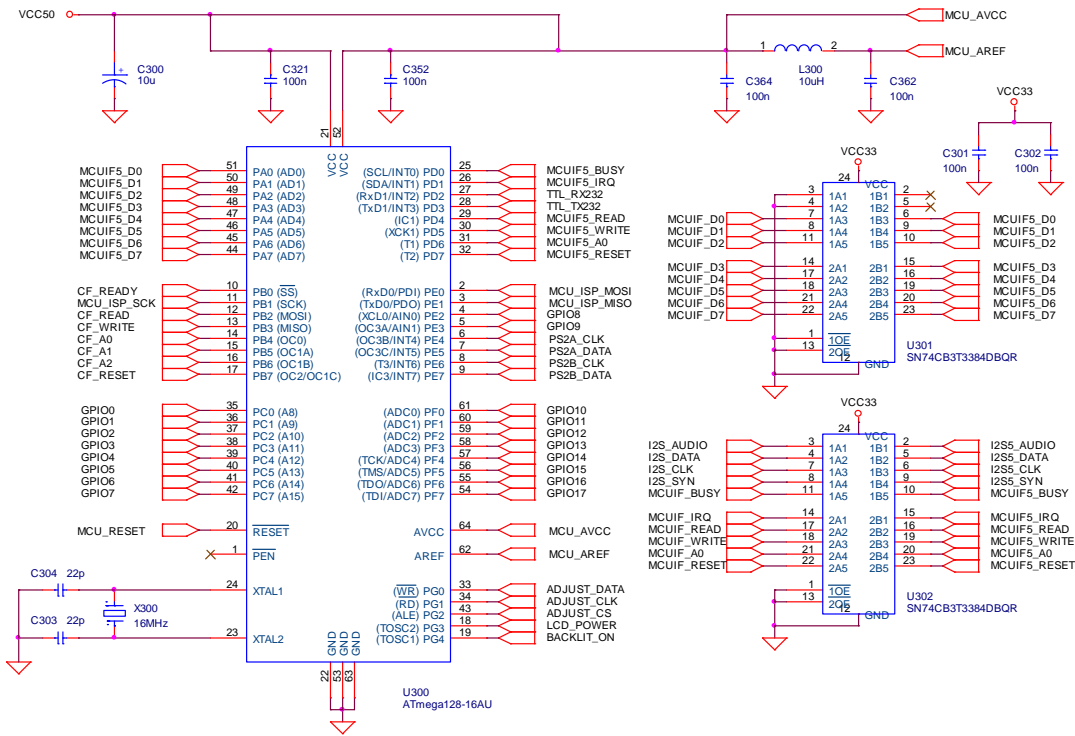


Fig.21: MCU core system

## PS/2 ports

The dual PS/2 ports are operating at 5V. Usually used for keyboard and mouse.

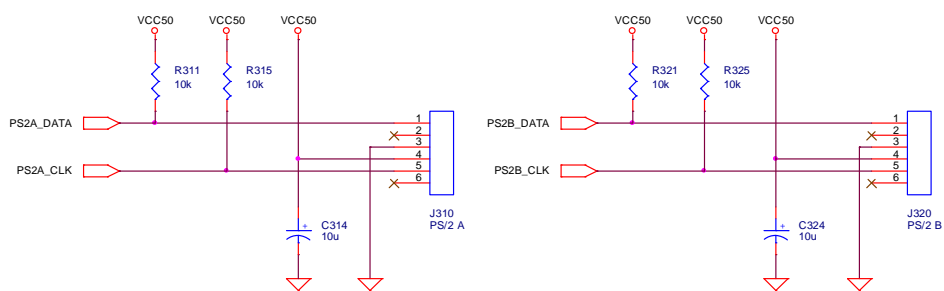


Fig.22: Dual PS/2 ports

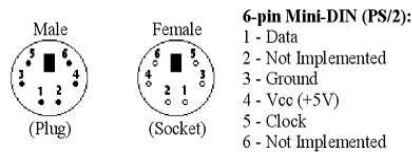


Fig.23: Pinout of the PS/2 connector

## RS232 serial port

A MAX232CWE chip is used for interfacing the TTL serial port signals from MCU with the RS232 world. The connector on the board is wired as a DTE device (DB9-M type).

For connection with a PC, a DB9 F-F cable with exchanged pins 2 and 3 is required.

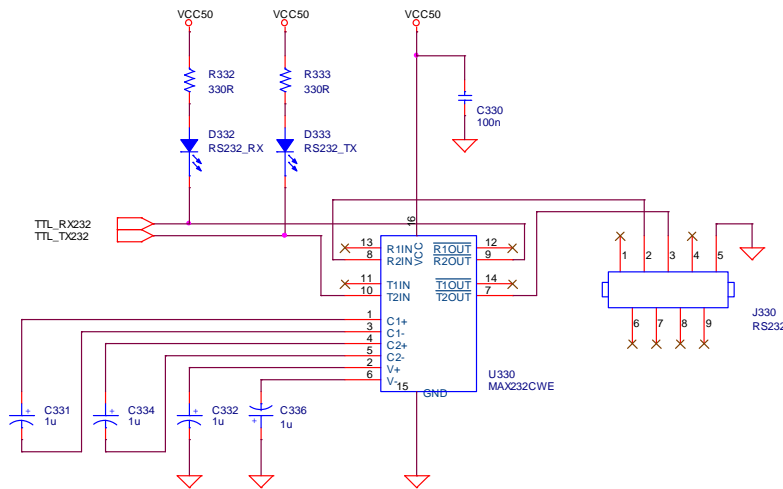


Fig.24: The RS232 interface

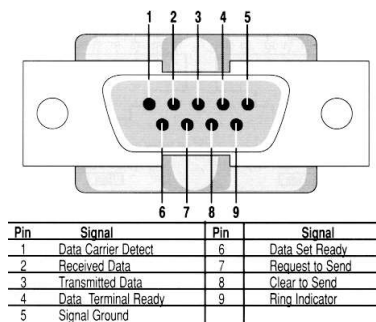


Fig.25: Pinout of the RS232 connector

## General purpose inputs/outputs - GPIO headers

There are 18 general purpose input/output lines and a 5.0V power source present on this GPIO header. Additionally a dedicated regulated power supply is wired here too. Besides the main connector, two smaller variants are present too. These have only one selectable power supply.

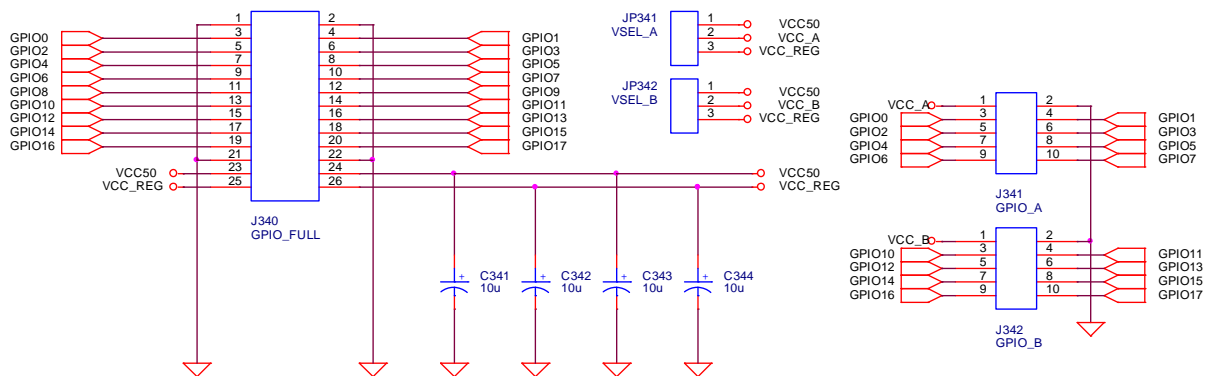


Fig.26: The GPIO headers



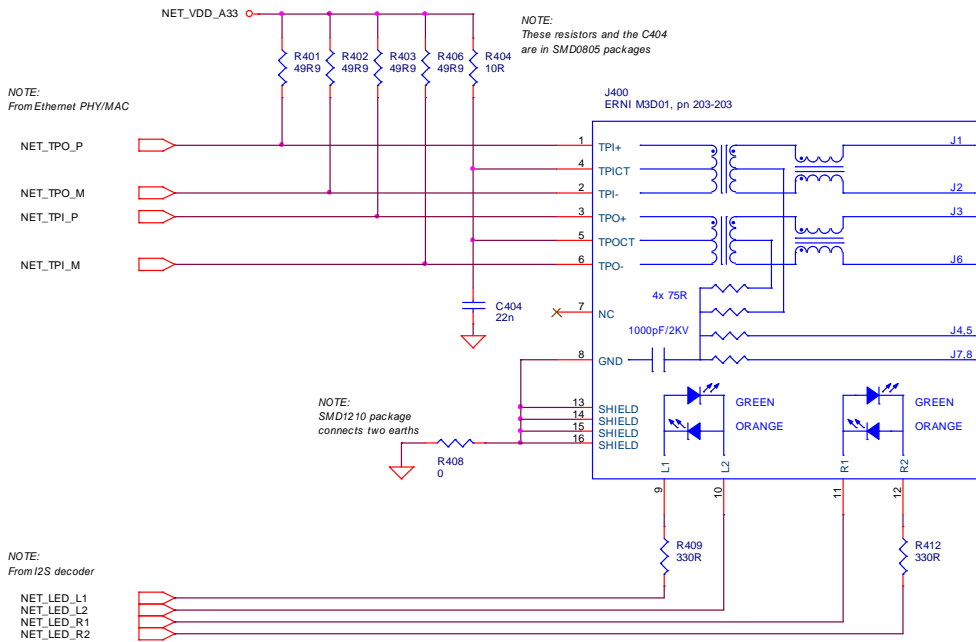


Fig.29: The RJ45 connector with integrated magnetics

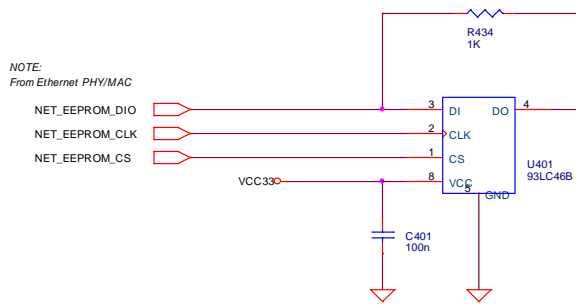


Fig.30: Network configuration EEPROM

## Display module

### Power switching

Both the 3.3V and 5.0V lines are switched because the display controller board does not know if the panel is using one or another voltage for powering itself. Signal controlled by MCU.

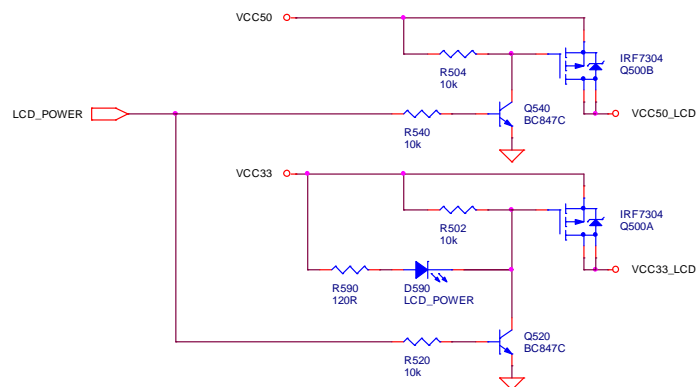


Fig.31: Switch for the LCD panel's power line

### Backlit on/off indicator

Controlled by the MCU.

Backlit on/off signal is created fully by the MCU.

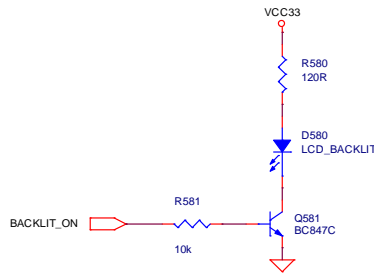


Fig.32: Backlit on/off indicator

### Backlit brightness adjustment

Controlled by the MCU.

Digitally controlled resistance is used to control the brightness of the CCFL.

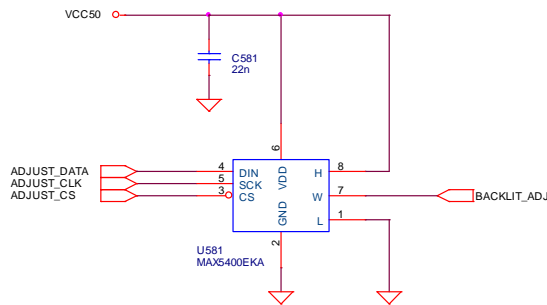


Fig.33: Digitally controlled resistor for brightness adjustment

### LVDS transmitter

This transmitter converts the parallel (TTL RGB) input to serial (LVDS) output.

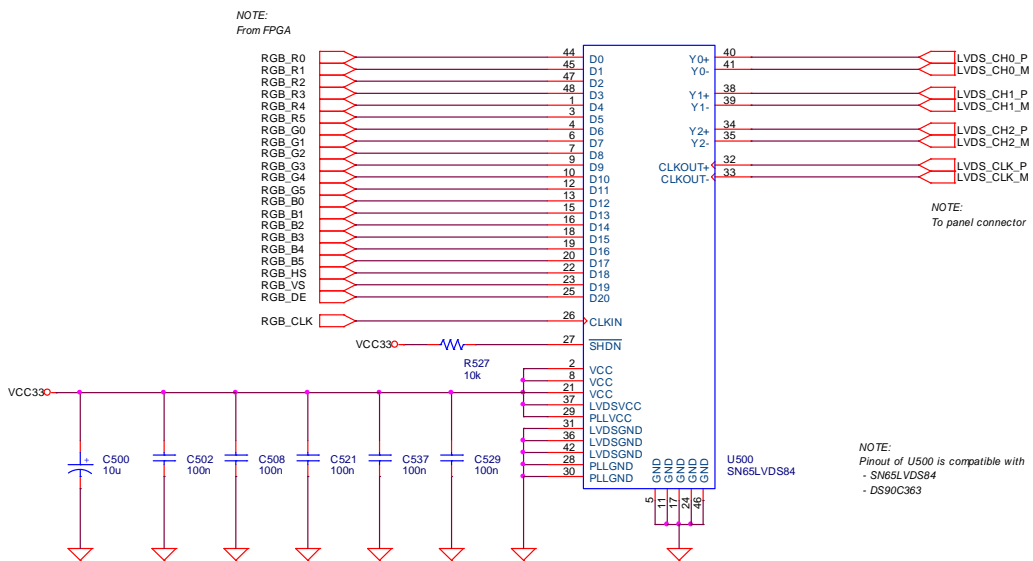


Fig.34: An 18-bit LVDS transmitter with decoupling capacitors

### LCD panel ports

The output headers provides both 3.3V and 5V for use as the LCD panel power thus the selection of the proper voltage is made by proper wiring of the cable from the controller board to the LCD panel.

### RGB TTL type

Uses a 40 pin header (2x20 pins)

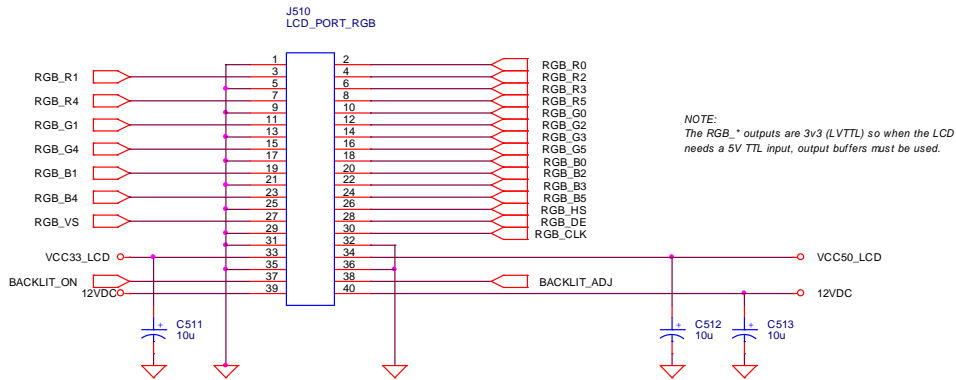


Fig.35: Connector for RGB TTL panels

### LVDS type

Uses a 34 pin header (2x17 pins)

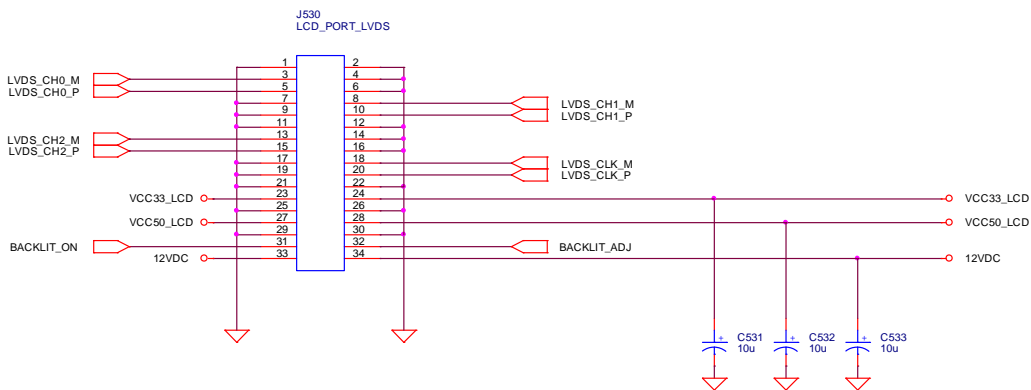


Fig.36: Connector for LVDS panels

## Memory card

There is a CF card socket which is wired to operate in a true IDE mode at 8bit. The data bus is shared with the MCU-FPGA interface so that the data exchange can save a cycle on each byte.

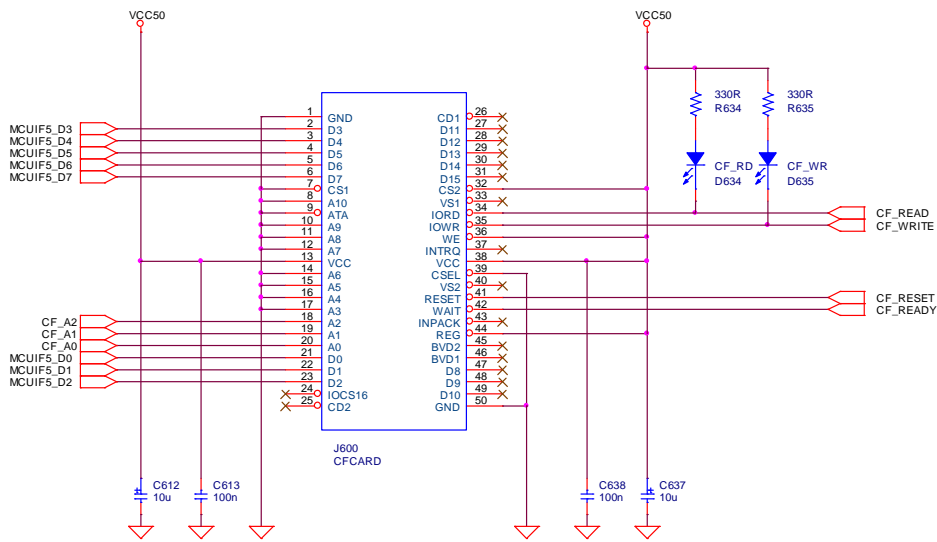


Fig.37: Compact flash socket

## Main memory

There is 16MB memory on the board which is made from 2 chips - for wider data path (2x16=32bit). When operating at 133MHz, the peak transfer rate of the memory system is 533MB/s.

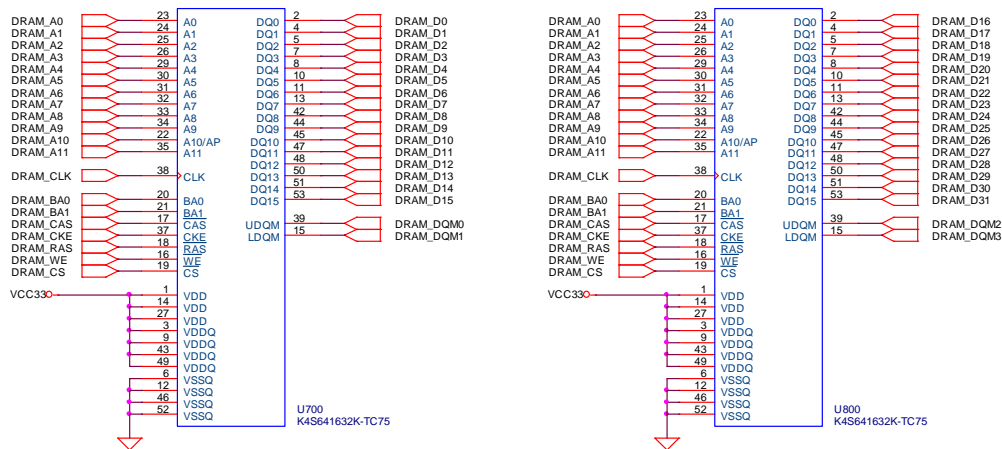


Fig.38: The two memory chips

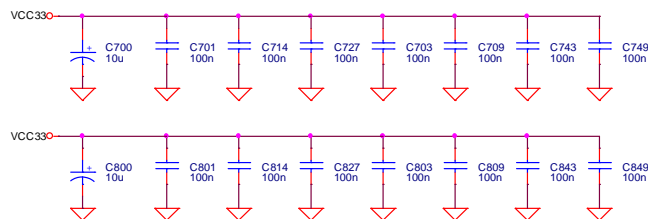


Fig.39: Decoupling capacitors for each power pin of memory

## I2S bus

The I2S bus is originated in the FPGA and goes through a level modifier (shown in MCU CORE picture) because both I2S devices (DAC and the deserializer) are for 5V. For this reason, some pull-up resistors are present on the board.

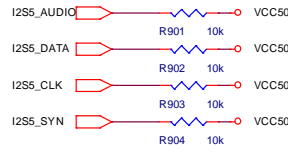


Fig.40: I2S bus pullups

## I2S audio decoder

The primary I2S channel is for audio output using a low cost DAC - MAX5556. The analog audio outputs are present as a pair of CINCH connectors and also on a 4 pin CDRUM style header.

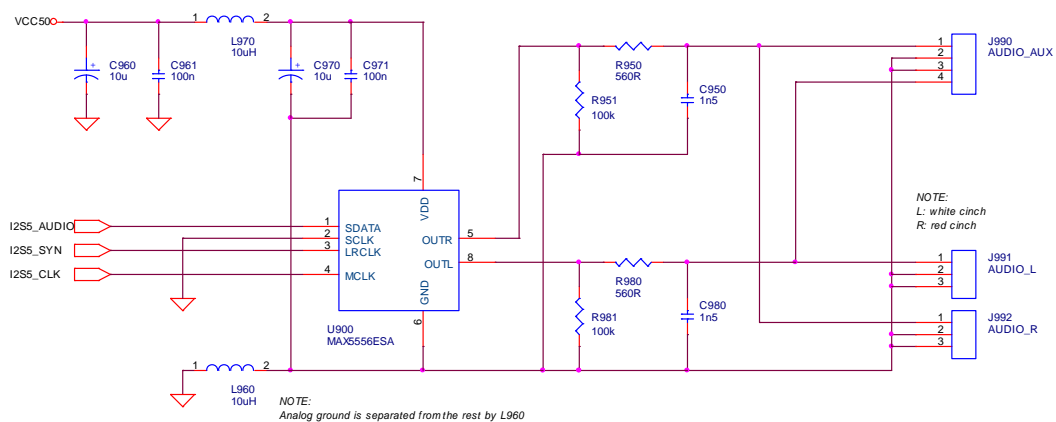


Fig.41: I2S audio decoder

## I2S data decoder

### Data decoder

The decoder translates the serial I2S input to parallel 32 bit output. Four signals are used for the RJ45 LEDs and another 4 for general purpose LEDs. The rest is then wired to GPO headers.

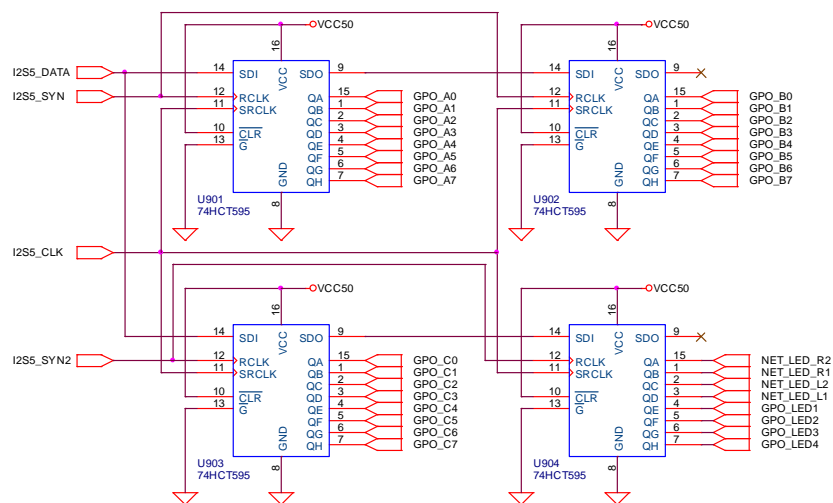


Fig.42: Deserializer for the second I2S channel

To make use of the second channel data, a simple inverter is made from one transistor:

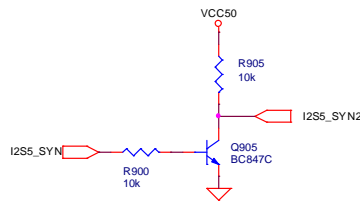


Fig.43: Sync (channel select) wire inverter

The required decoupling capacitors are also present:

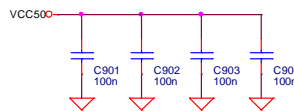


Fig.44: Decoupling

### General purpose LED's

These four LEDs are controlled indirectly through the I2S bus and can be used to indicate internal states in the FPGA.

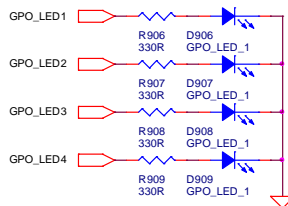


Fig.45: General purpose LEDs

### General purpose outputs - GPO headers

These output headers have a 5.0V power line on their first pin, then 8 bits of output and a ground. They are separated for easy use with multiple external indicators or other output devices.

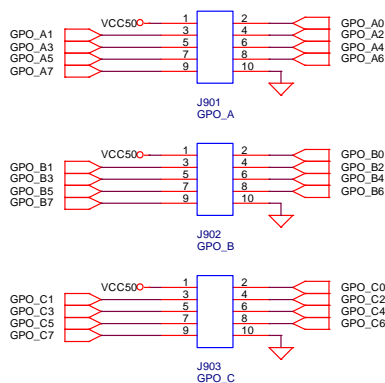


Fig.46: Three headers for general purpose outputs

## Programming

### JTAG for FPGA

This JTAG header is designed for easy use with the programmer from trenz-electronic.

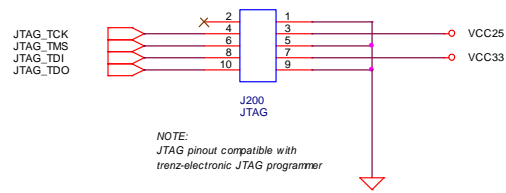


Fig.47: JTAG header

### AVRISP for MCU

This AVRISP header is designed for use with the original AVRISP programmer from Atmel.

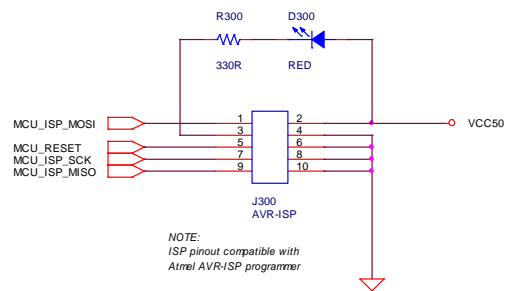


Fig.48: AVR ISP header

## Initialization

### Configuration Reload button

By pressing this button, the FPGA is loaded with the configuration stored in the *Platform flash* (PROM) device.

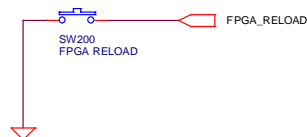


Fig.49: FPGA reload configuration button

### Reset button for MCU

This button restarts the microcontroller and the RC circuit provides also the power-on reset.

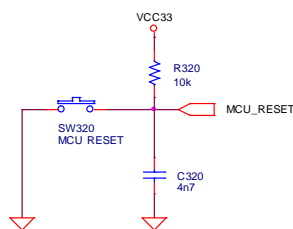


Fig.50: MCU reset button